

# Fonseca 14 UMA Schematics Document

## rPGA988A Mobile Arrandale

### Intel Ibex Peak-M

2010-03-19

[www.aitech1.ru](http://www.aitech1.ru)  
REV : -1

*DY : Nopop Component  
B\_TPM:Use Lom TPM  
C\_TPM:Use China TPM*

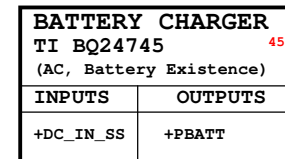
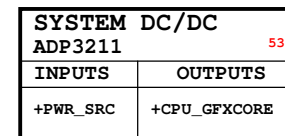
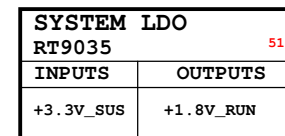
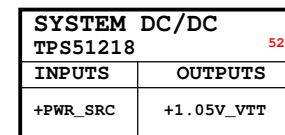
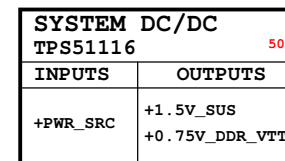
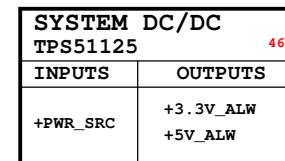
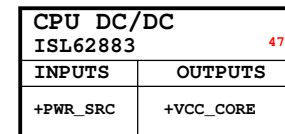
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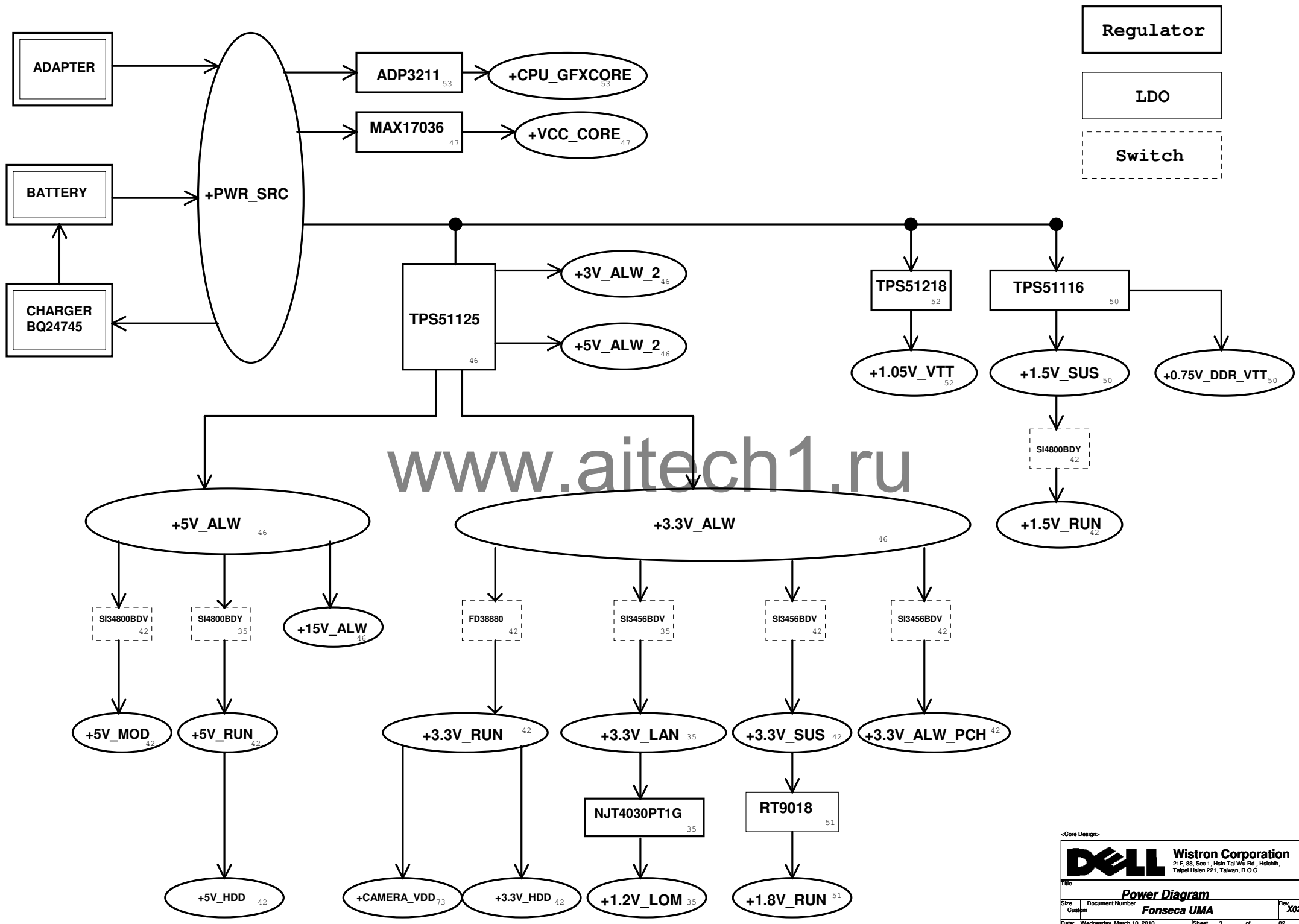


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	<b>DF3-14</b>
<b>Project code</b>	91.4GN01.001
<b>PCB P/N</b>	48.4GN01.0SC
<b>Revision</b>	09276 - SC

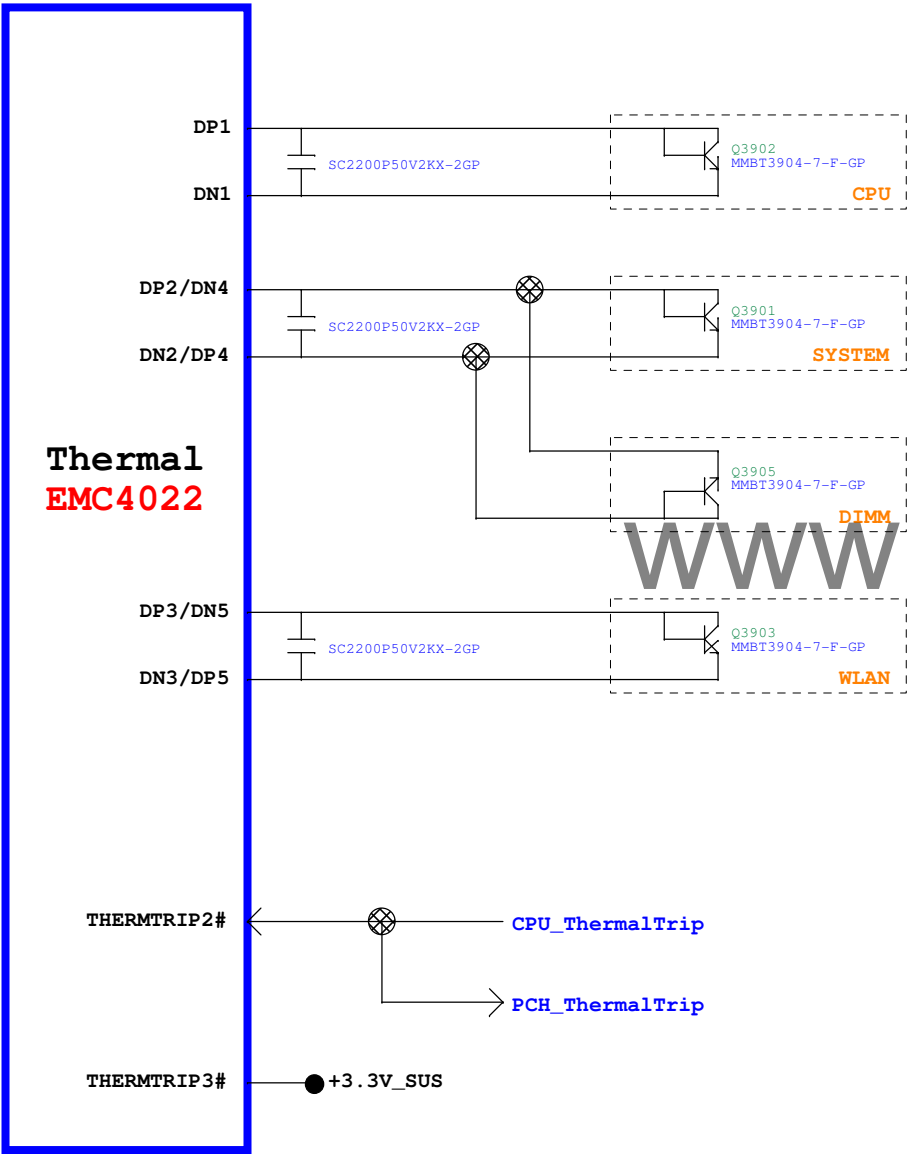




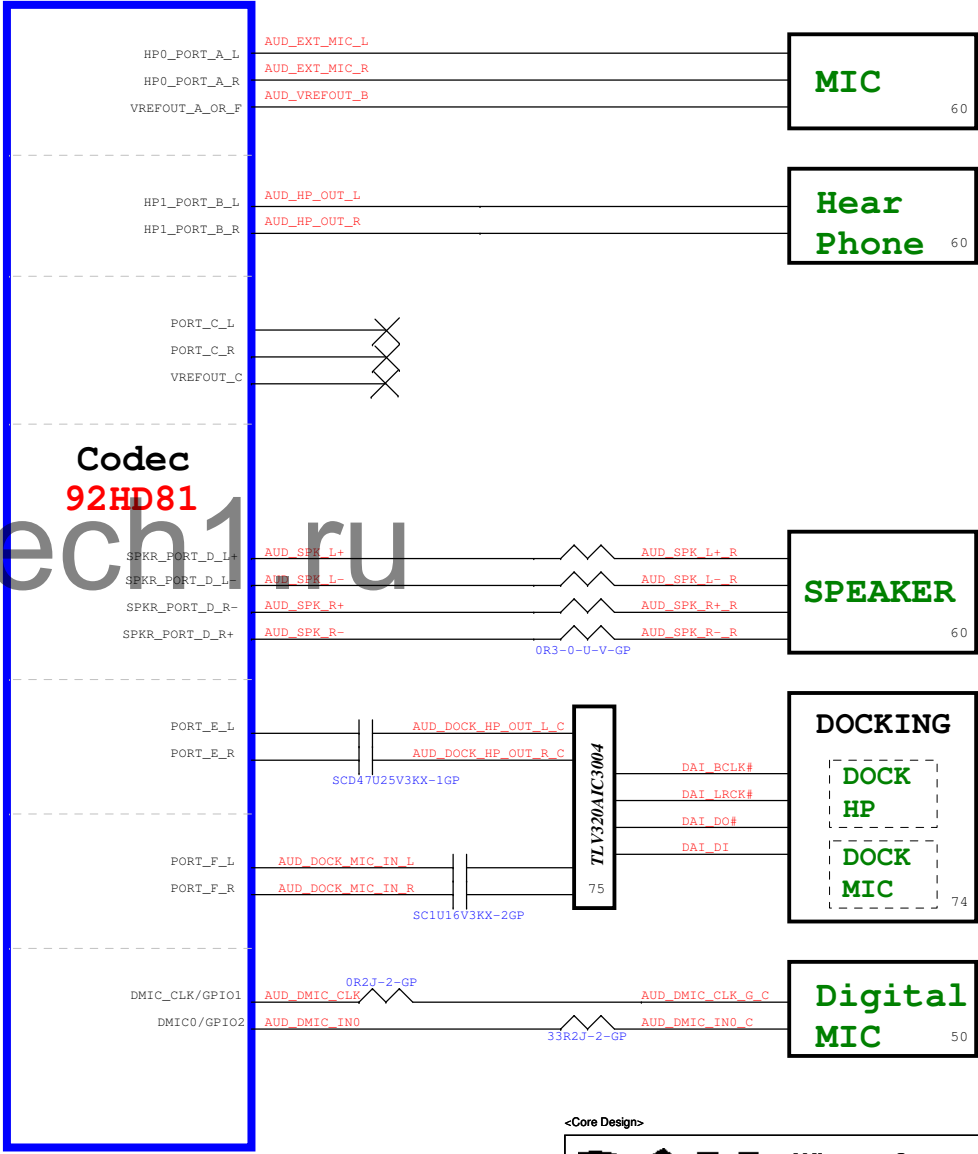




# Thermal Block Diagram



# Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> <b>Note:</b> Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b> <b>Note:</b> CRB uses a 330-k resistor.
GNT0#, GNT1#	<b>Default (SPI):</b> Leave both GNT0# and GNT1# floating. No pull up required <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.  <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default</b> - Internal pull-up. <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	<b>Enable Intel Anti-Theft Technology:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Intel Anti-Theft Technology:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Intel Anti-Theft Technology:</b> Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] <b>Disable Intel Anti-Theft Technology:</b> Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. <b>High (1):</b> Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. <b>Note:</b> CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. <b>Note:</b> This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	<b>Default</b> = Do not connect (floating). Internal pull-up. <b>High(1)</b> = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. <b>Low (0)</b> = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1


## PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	Not available for HM55
LANE8	Not available for HM55

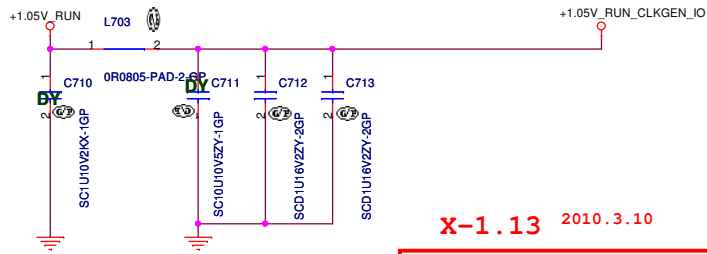
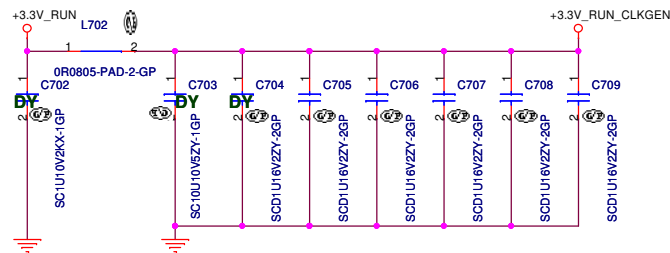
## USB Routing

USB	
Pair	Device
0	USB0 @ MB
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCKING PORT1
9	DOCKING PORT2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

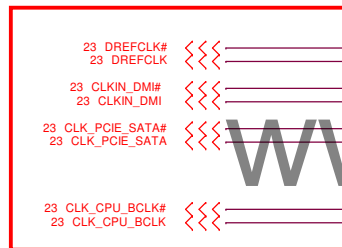
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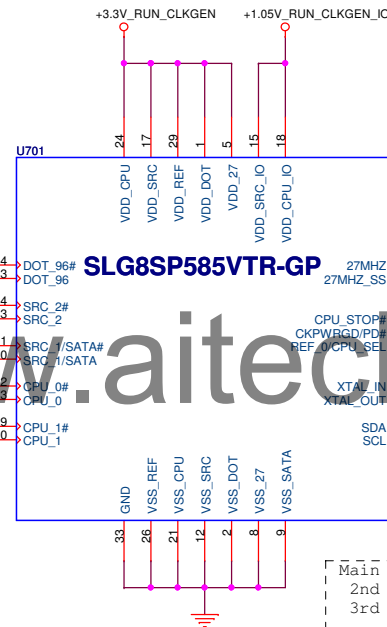
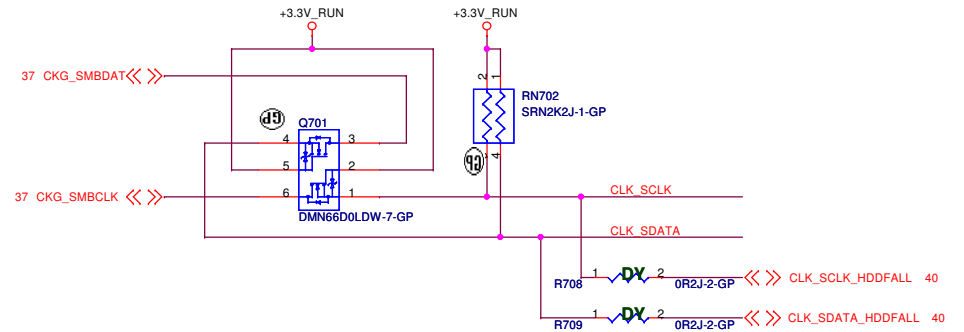
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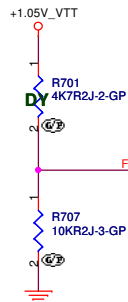
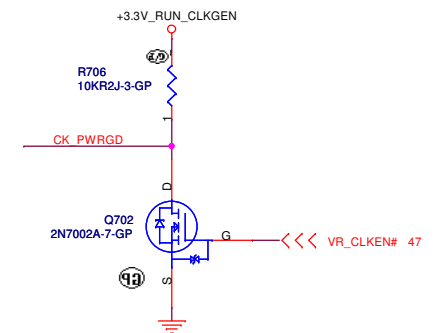
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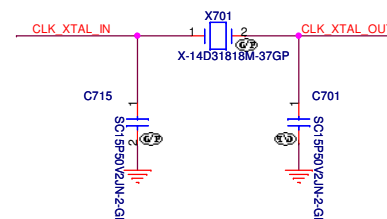
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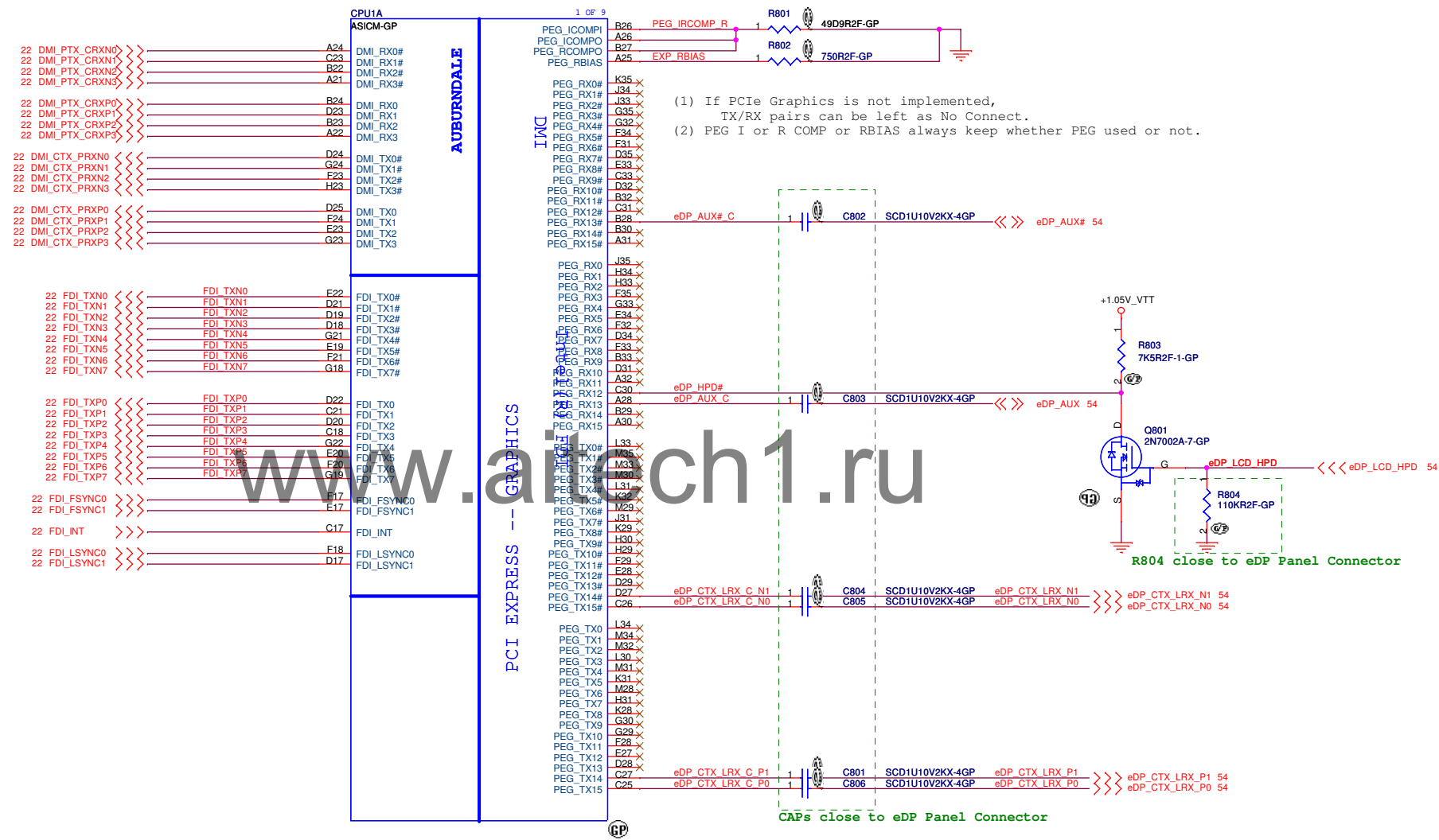


Main Source: 71.08585.003 (SLG8SP585VTR)  
2nd Source: 71.93197.003 (ICS9LRS3197AKLFT)  
3rd Source: 71.28748.A03 (SL28748ELCT)



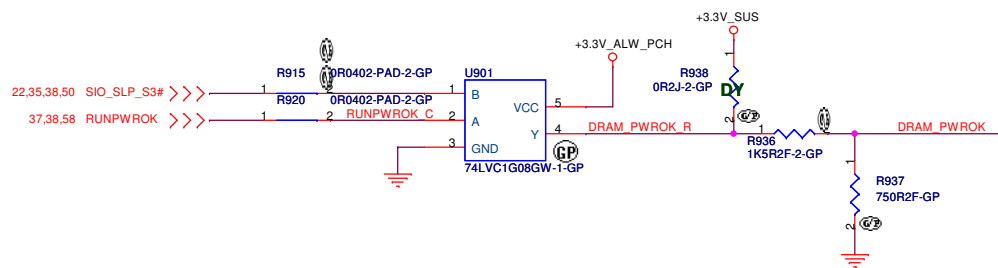
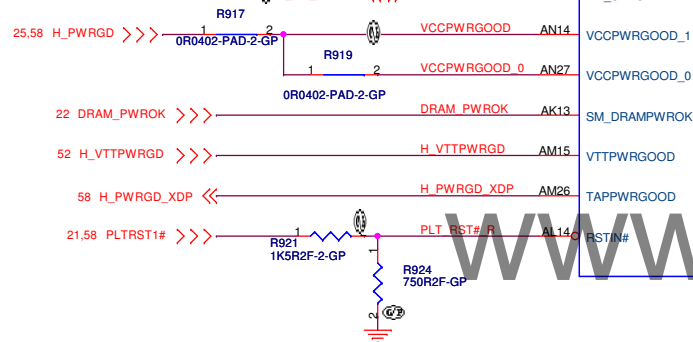
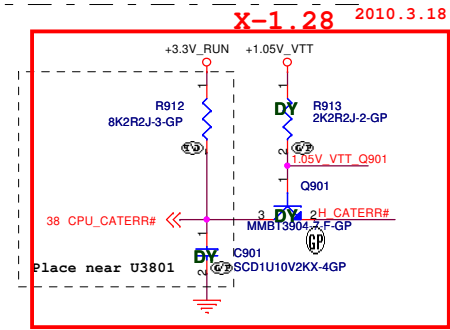
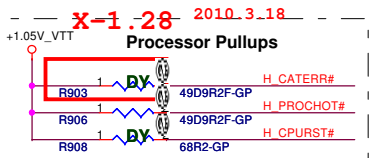
FSC	0	1
SPEED	133MHz (Default)	100MHz



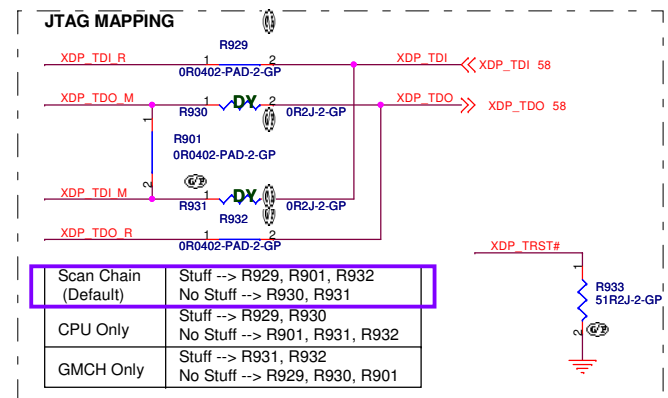
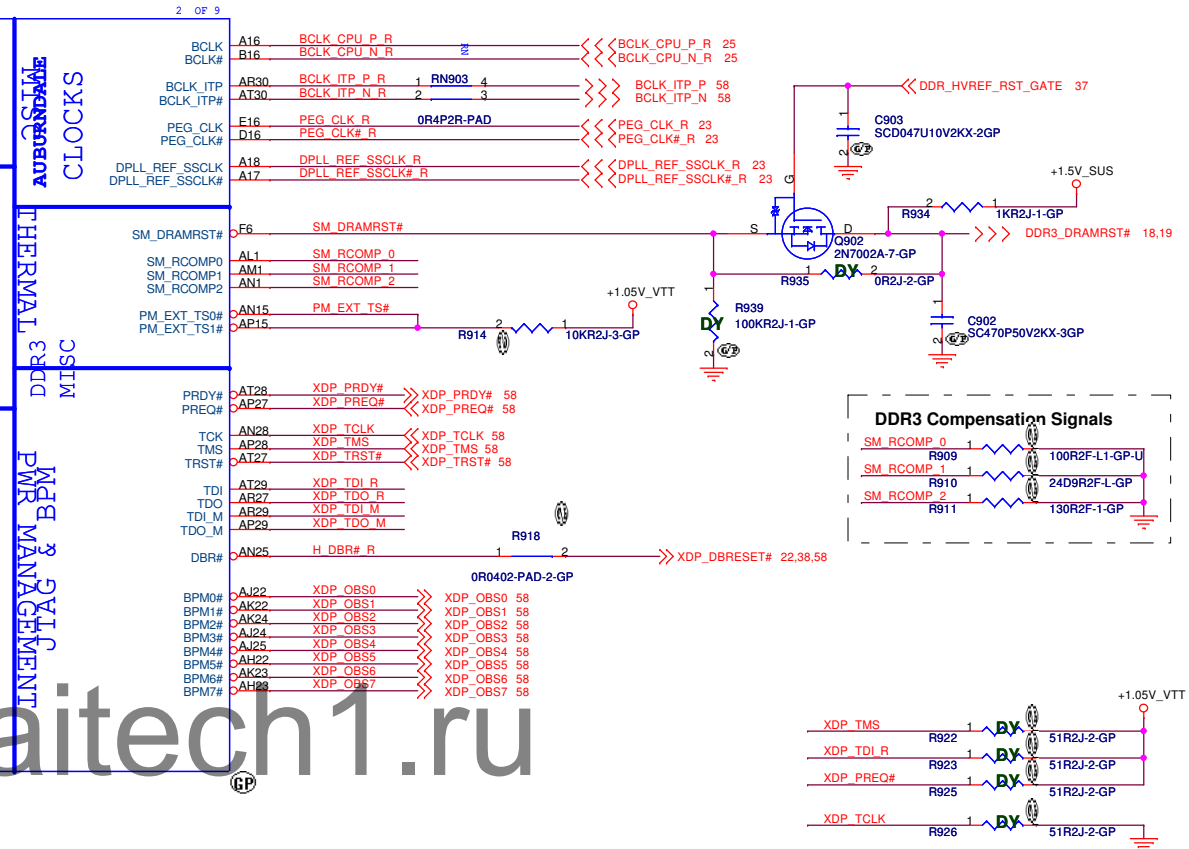


SSID = CPŮ

### Processor Compensation Signals



X01.09/0917



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CPU Thermal/Clock/PM (2/7)

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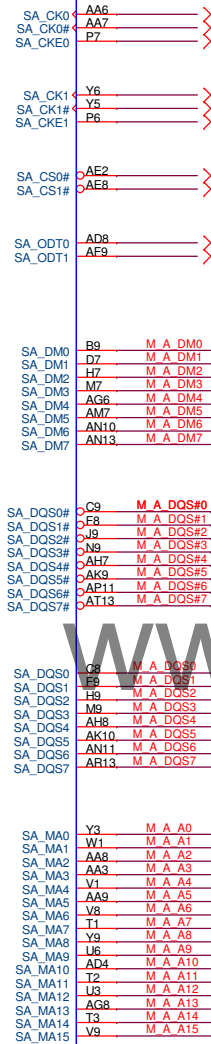
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ASICM-GP

AUBURNDALE

DDR SYSTEM MEMORY A

3 OF 9



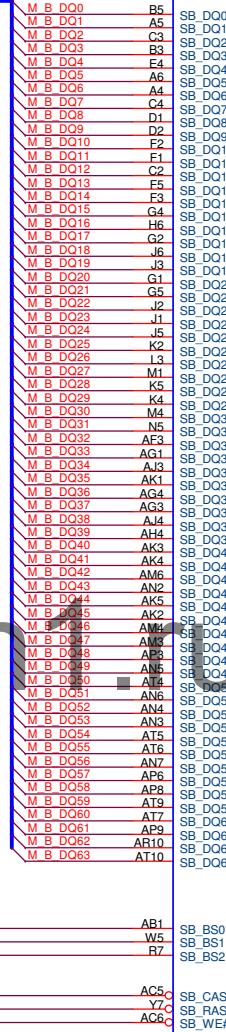
GP

CPU1D  
ASICM-GP

AUBURNDALE

DDR SYSTEM MEMORY - B

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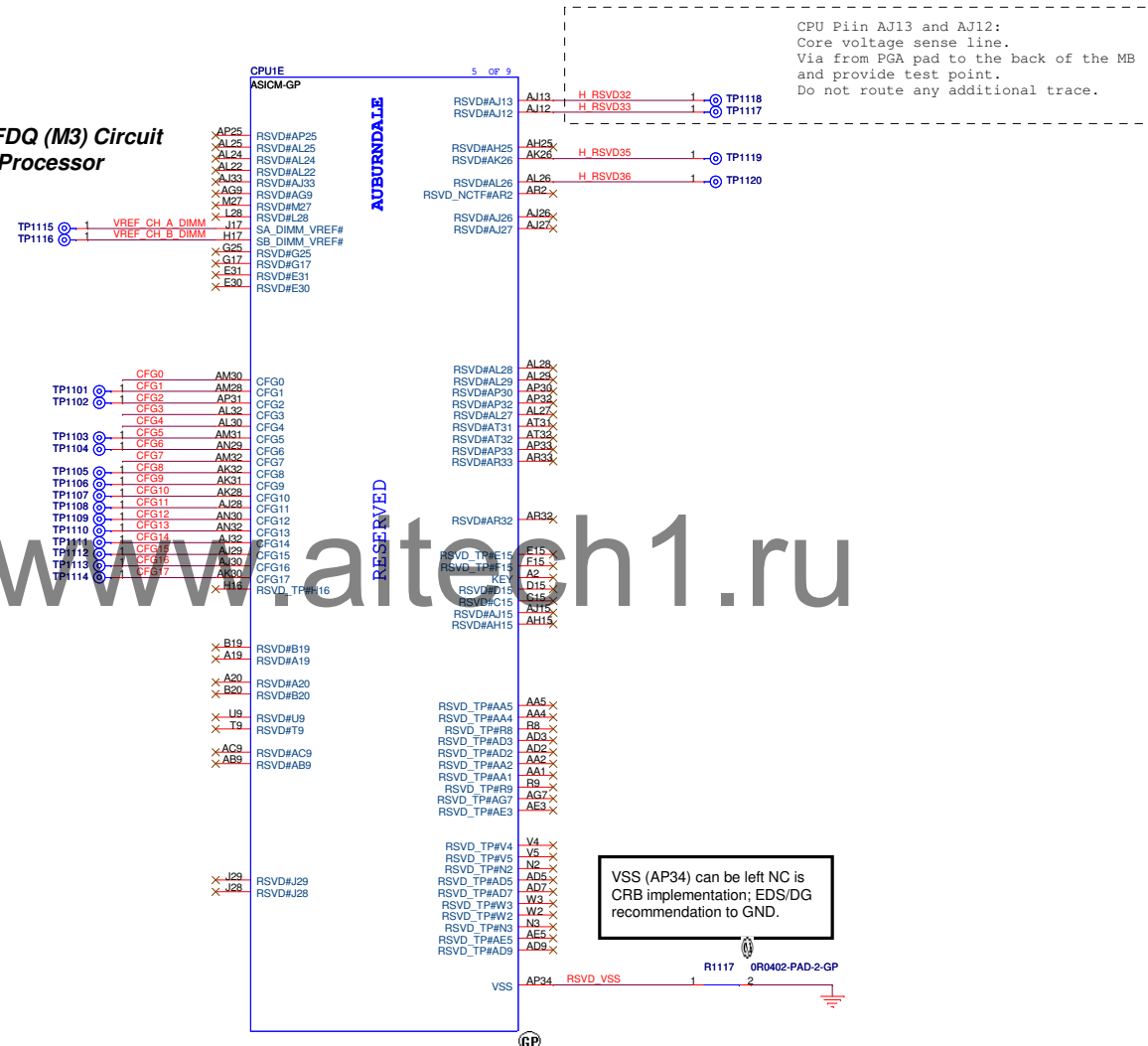
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Size: A3 Document Number: **Fonseca UMA** Rev: **X02**

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**SSID = CPU**

### ***SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor***



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled (Clarkfield only)

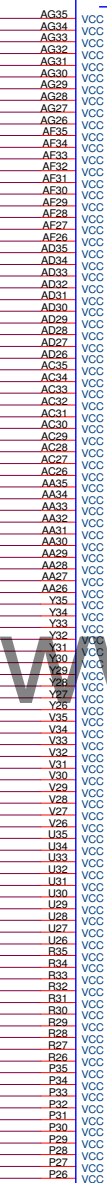
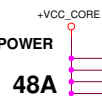
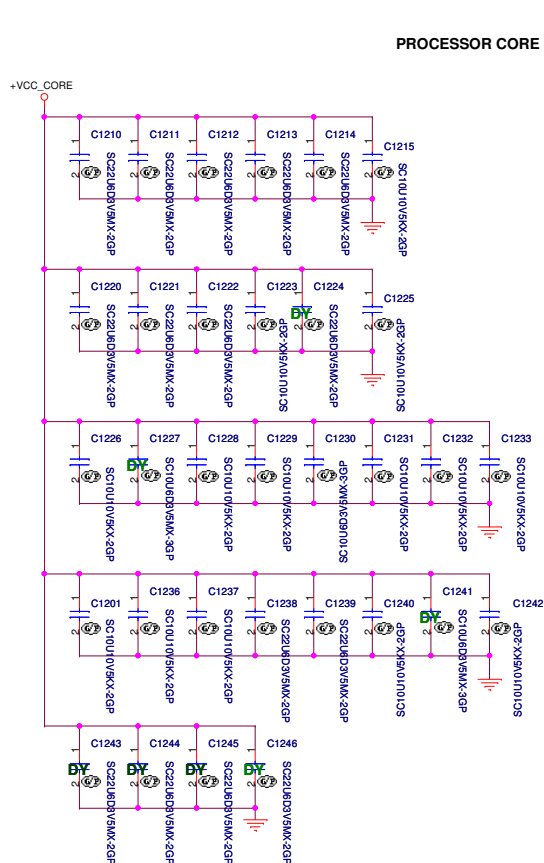
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port</p>

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (PGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>

VSS (AP34) can be left NC in CRB implementation; EDS/DG recommendation to GND.

**SSID = CPU**



**AUBURNDALE**

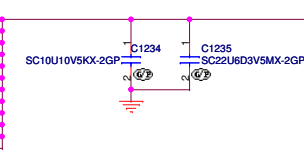
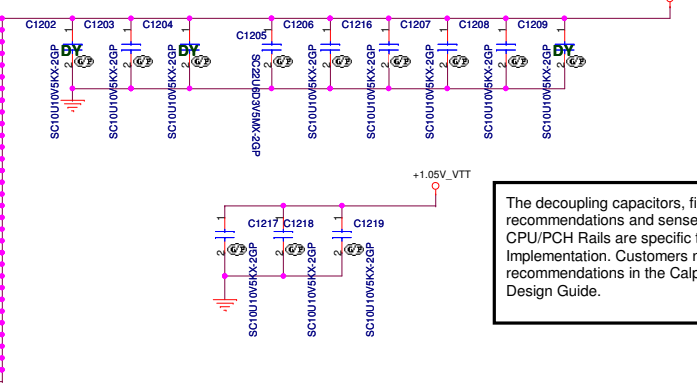
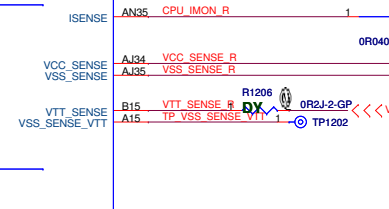
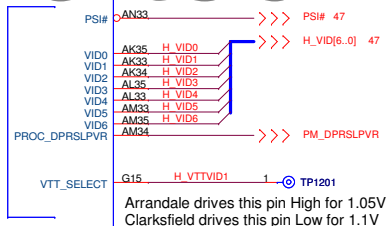
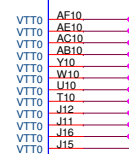
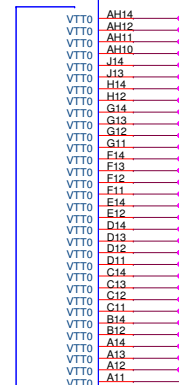
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CPU CORE SUPPLY

# POWER

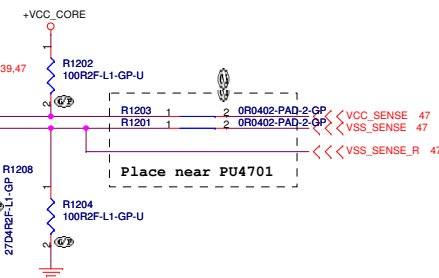
CPU VIDS

**SENSE LINES**



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that  
The VTT Rail values are  
Arrandale for VTT=1.05V  
Clarksfield for VTT=1.1V



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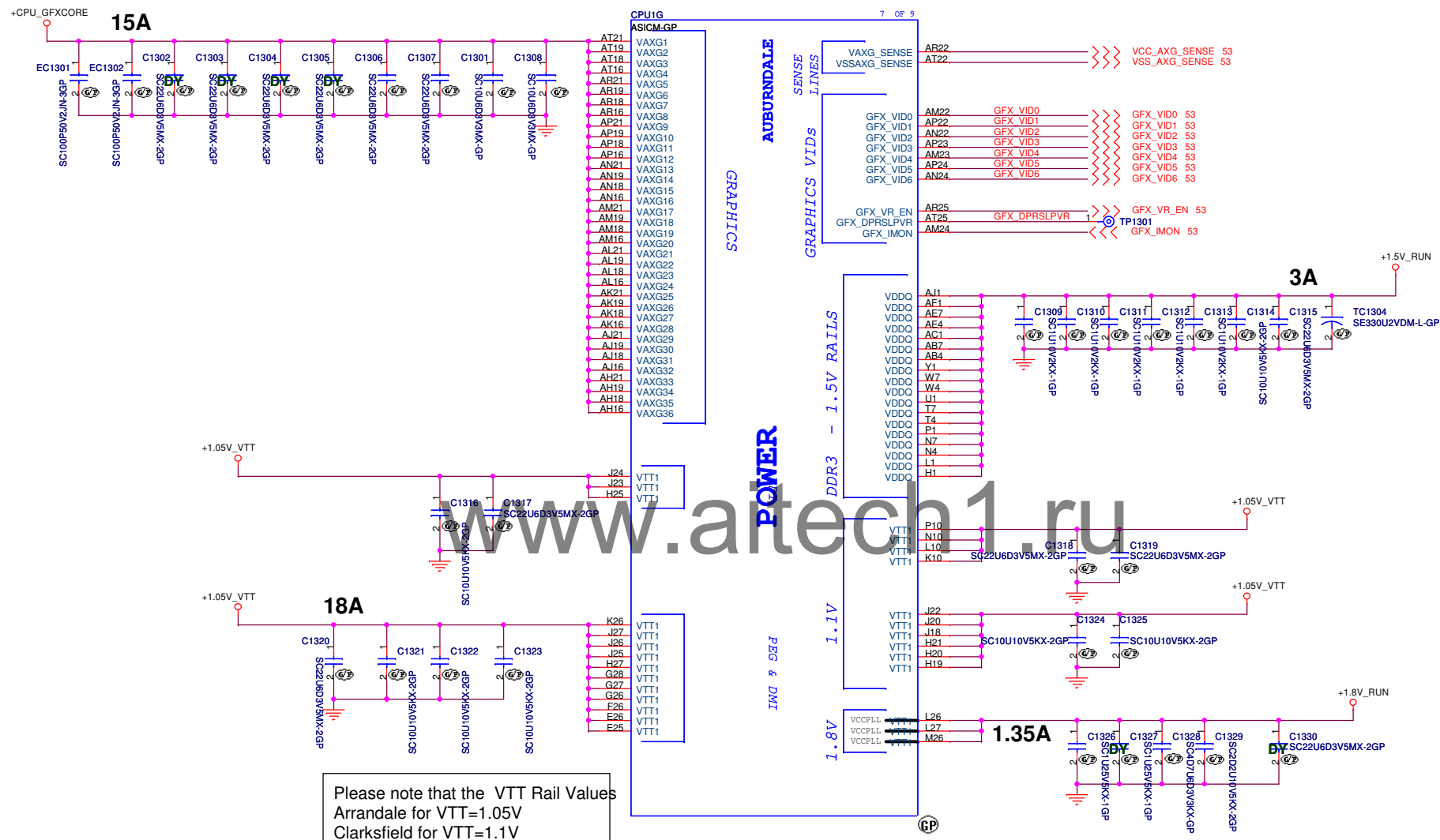


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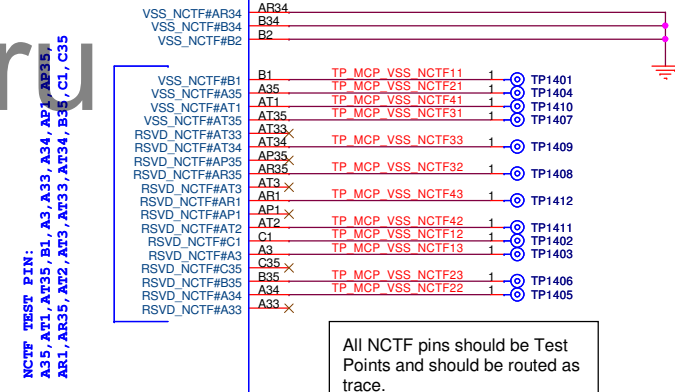
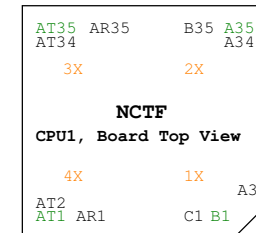
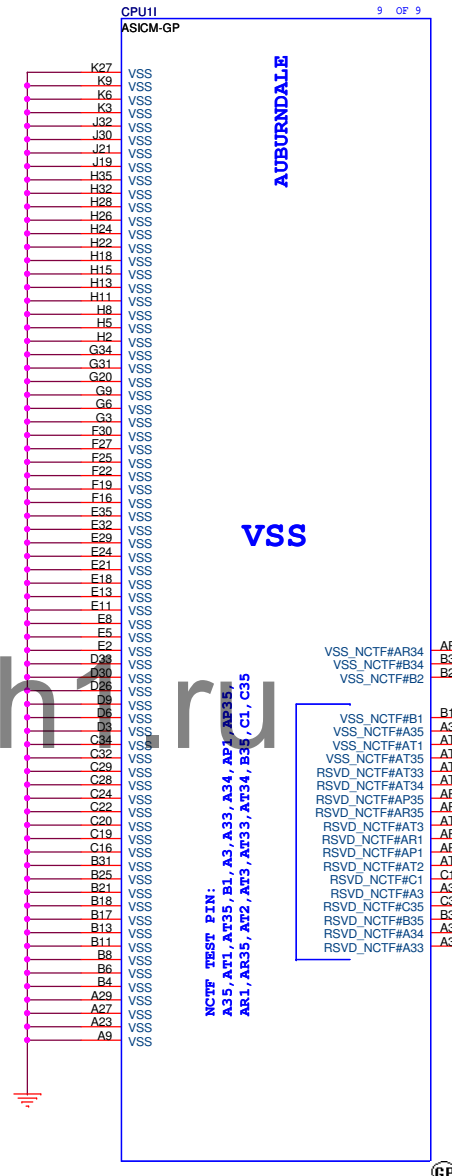
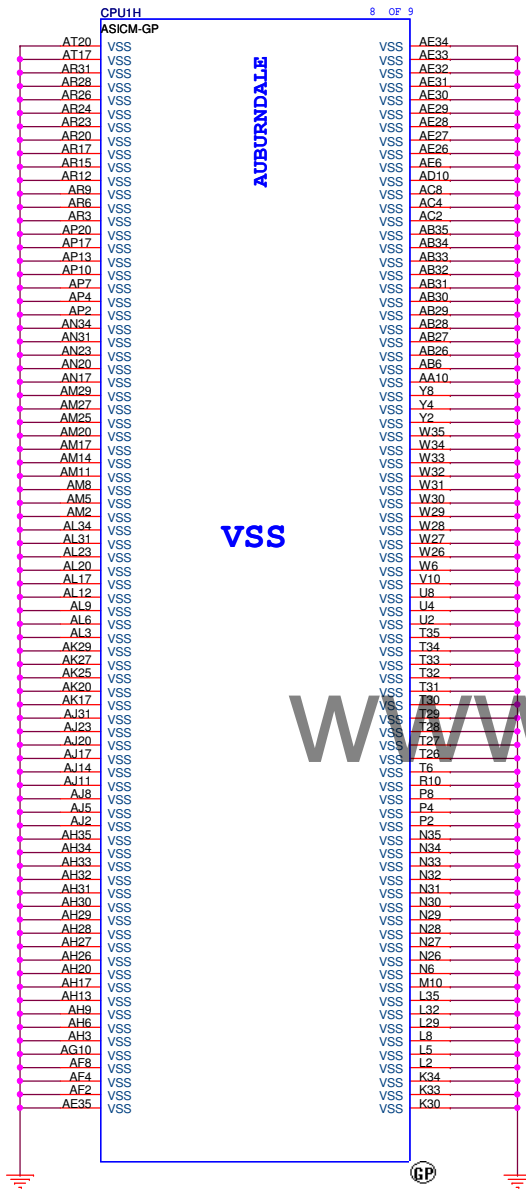


**SSID = CPU**



Please note that the VTT Rail Values  
Arrandale for VTT=1.05V  
Clarksfield for VTT=1.1V


SSID = CPU



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Document Number

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**Reserve**

**Fonseca UMA**

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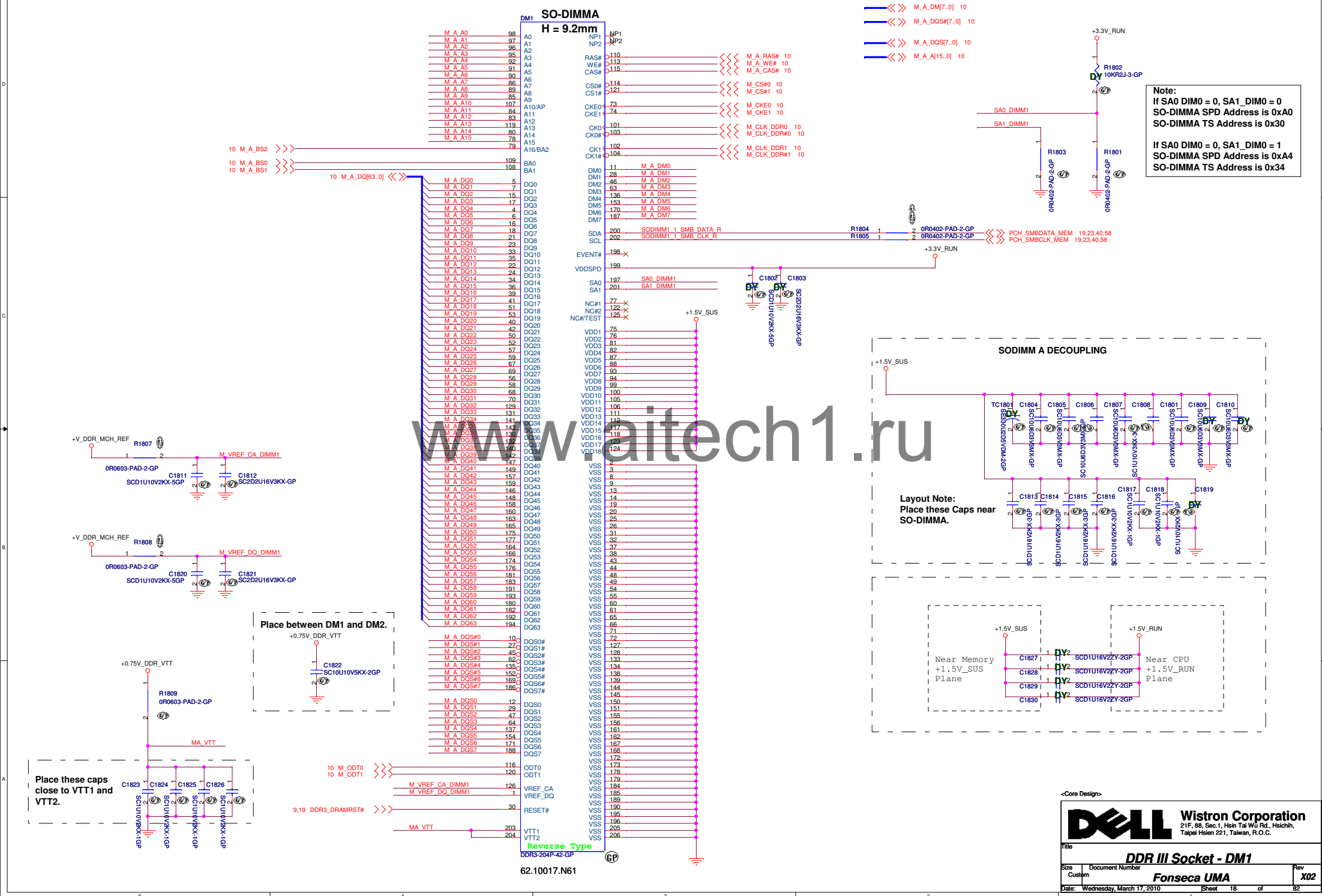
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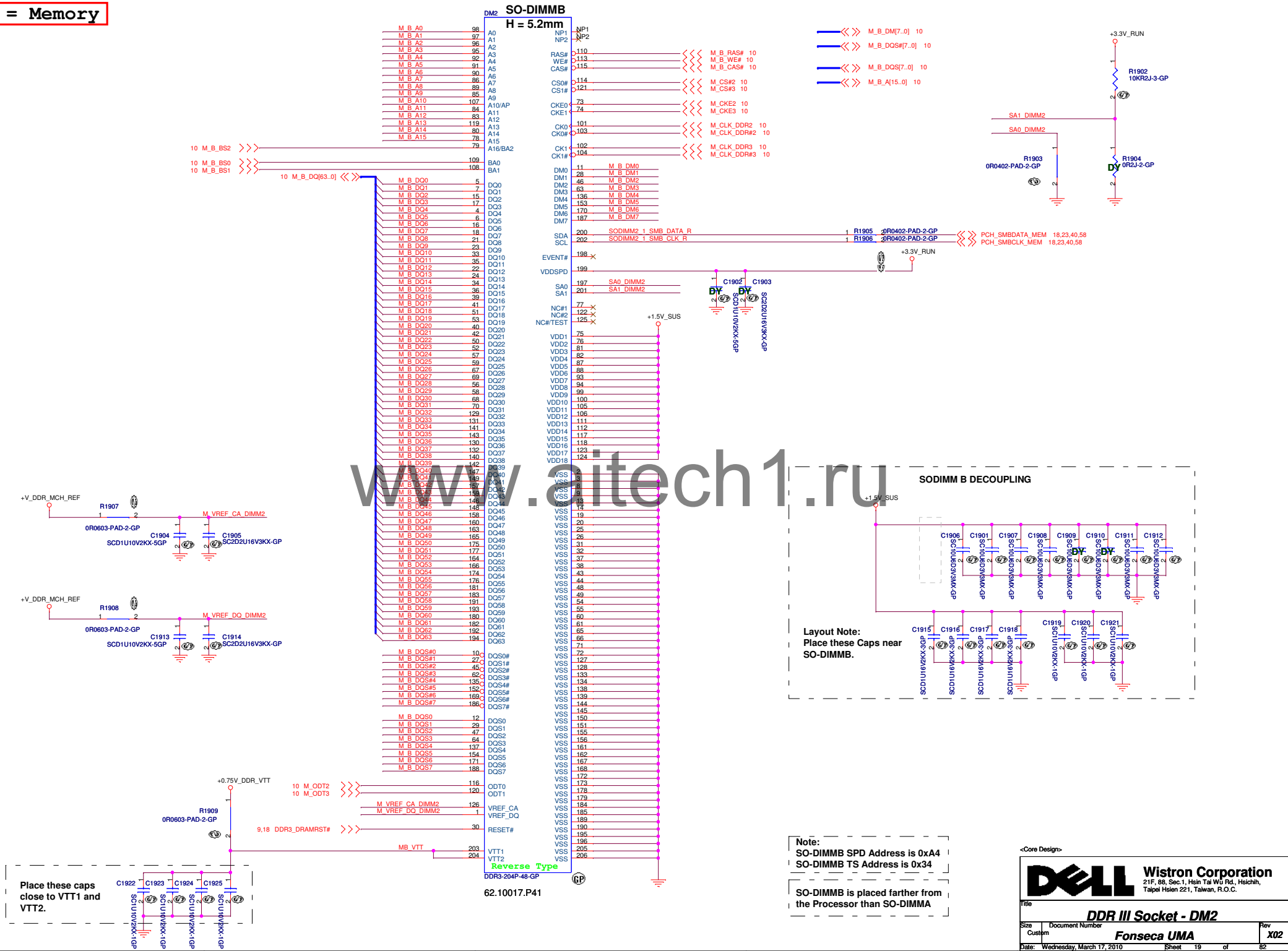
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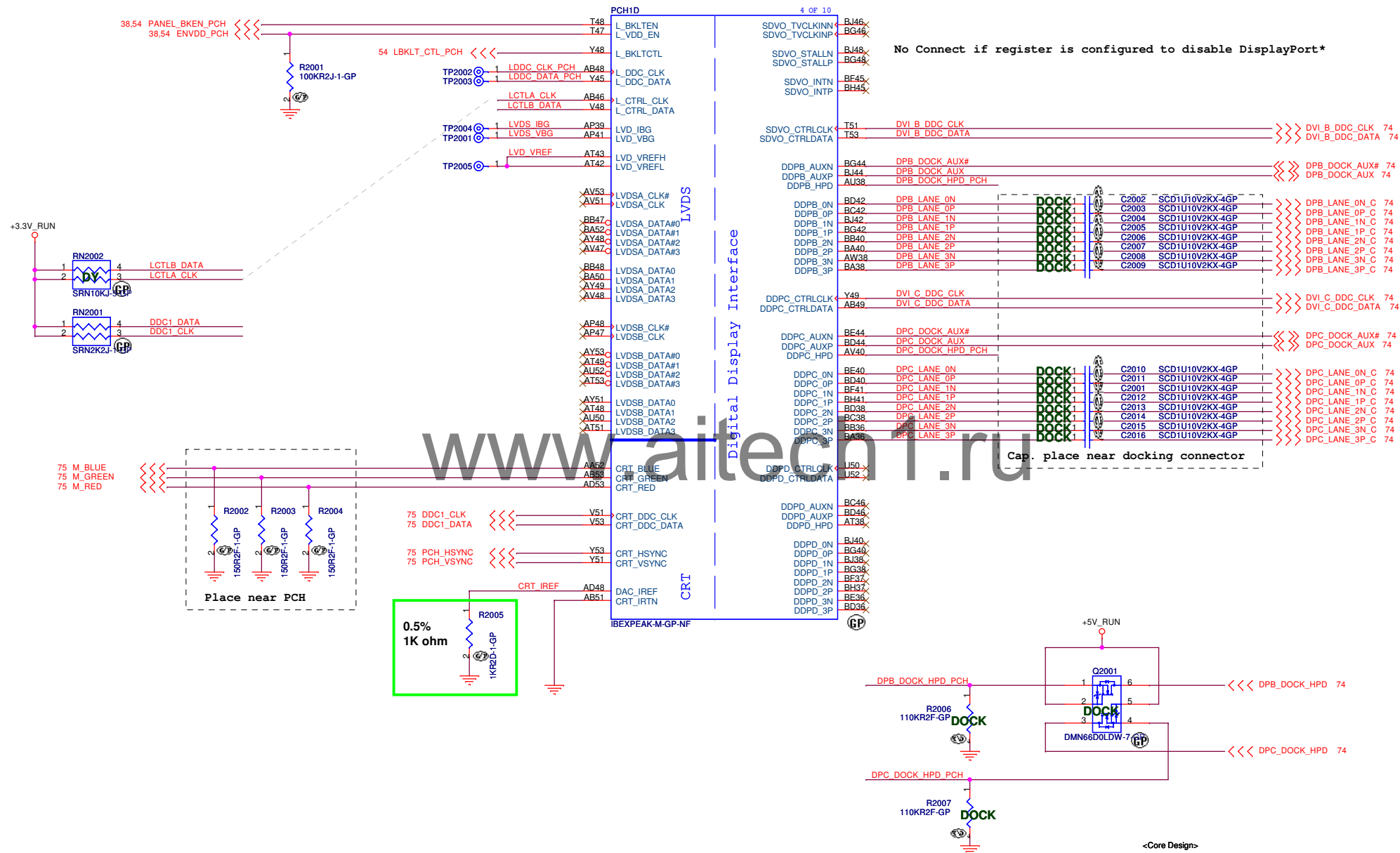
**SSID = Memory**



**SSID = Memory**



**SSID = PCH**



## <Core Design>



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Title

### PCH - LVDS/CRT/DDI (1/9)

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Rev  
**X02**

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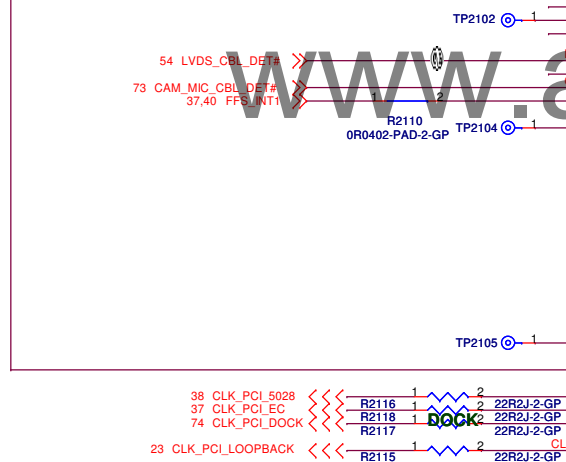
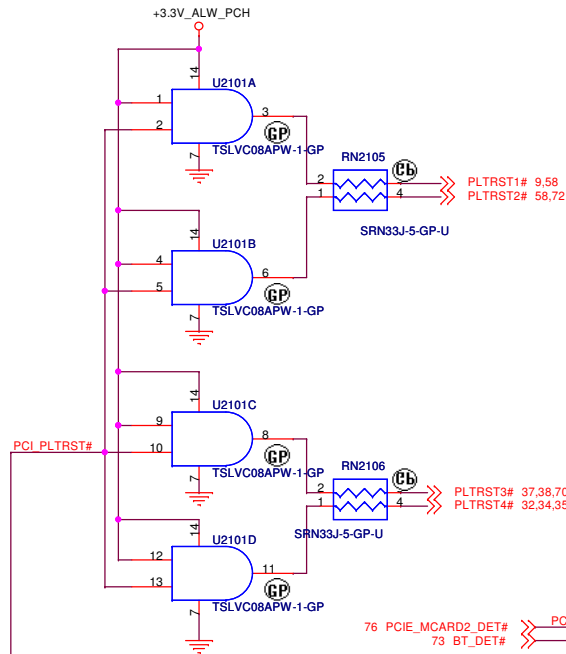
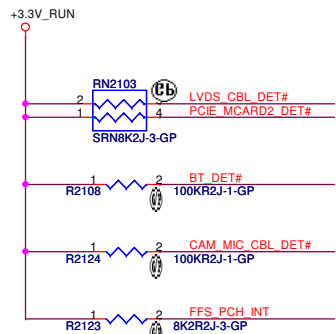
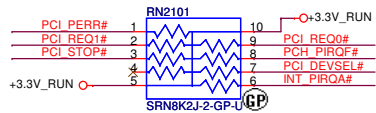
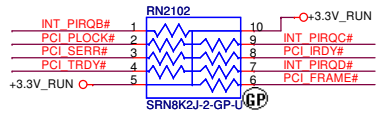
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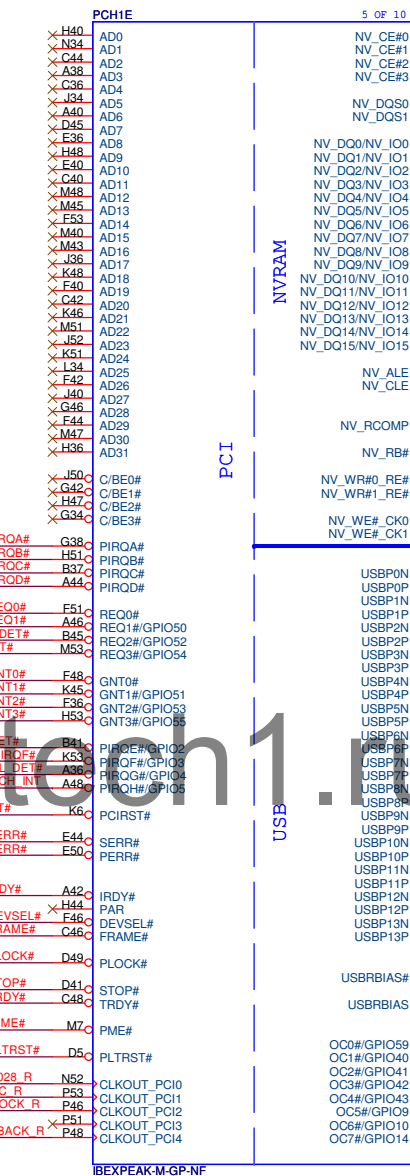
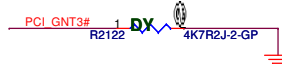


# SSID = PCH



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

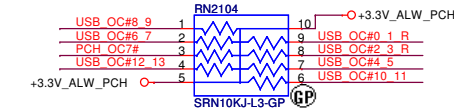
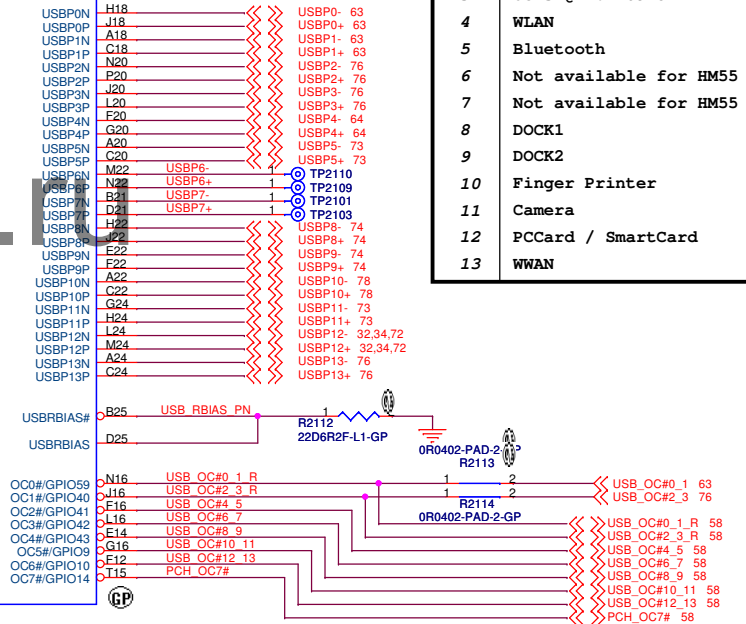
PCI\_GNT[3:0]#: Internal pull high during Strap



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Core Design>

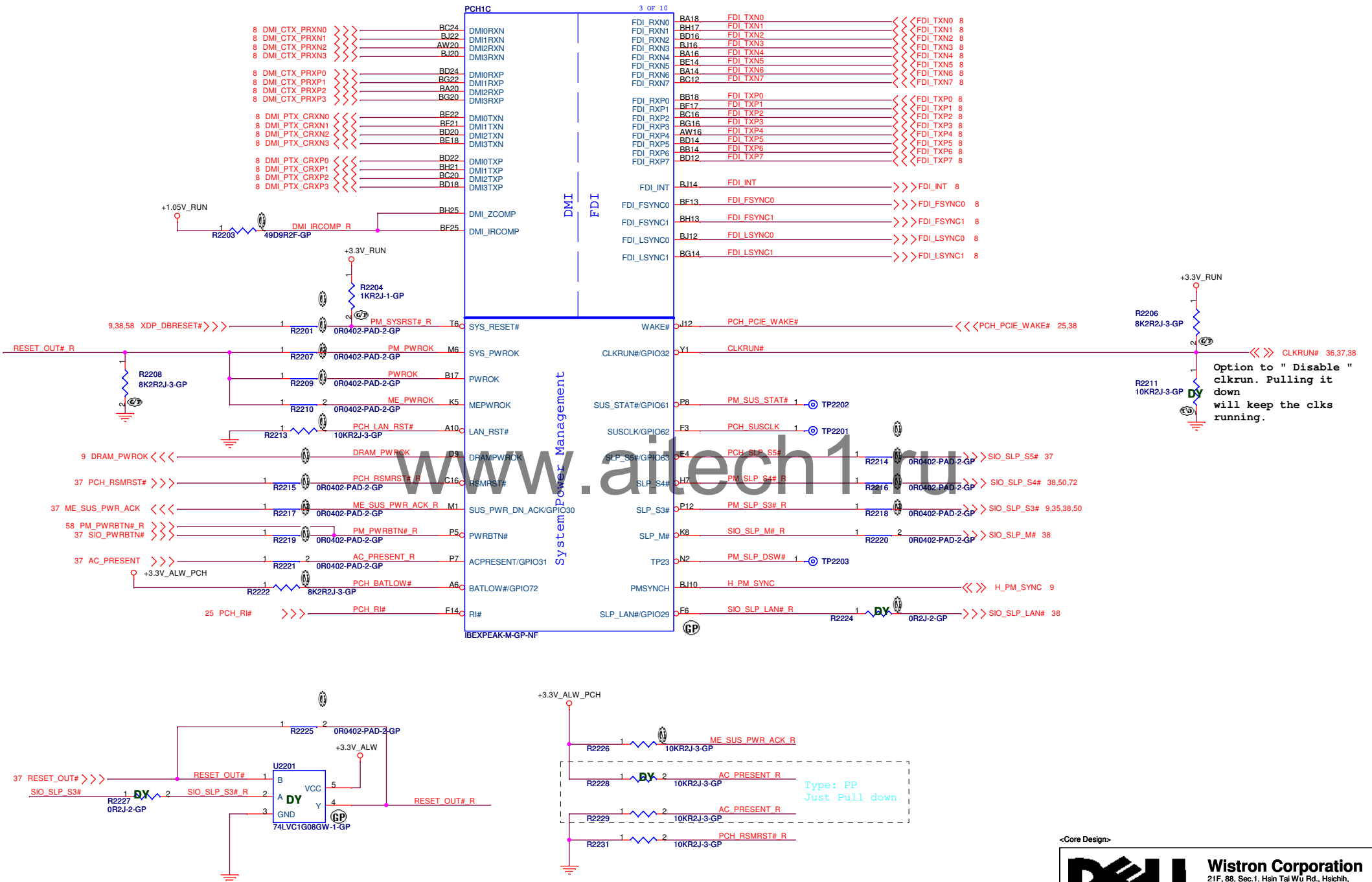
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH - PCI/USB/NVRAM (2/9)**

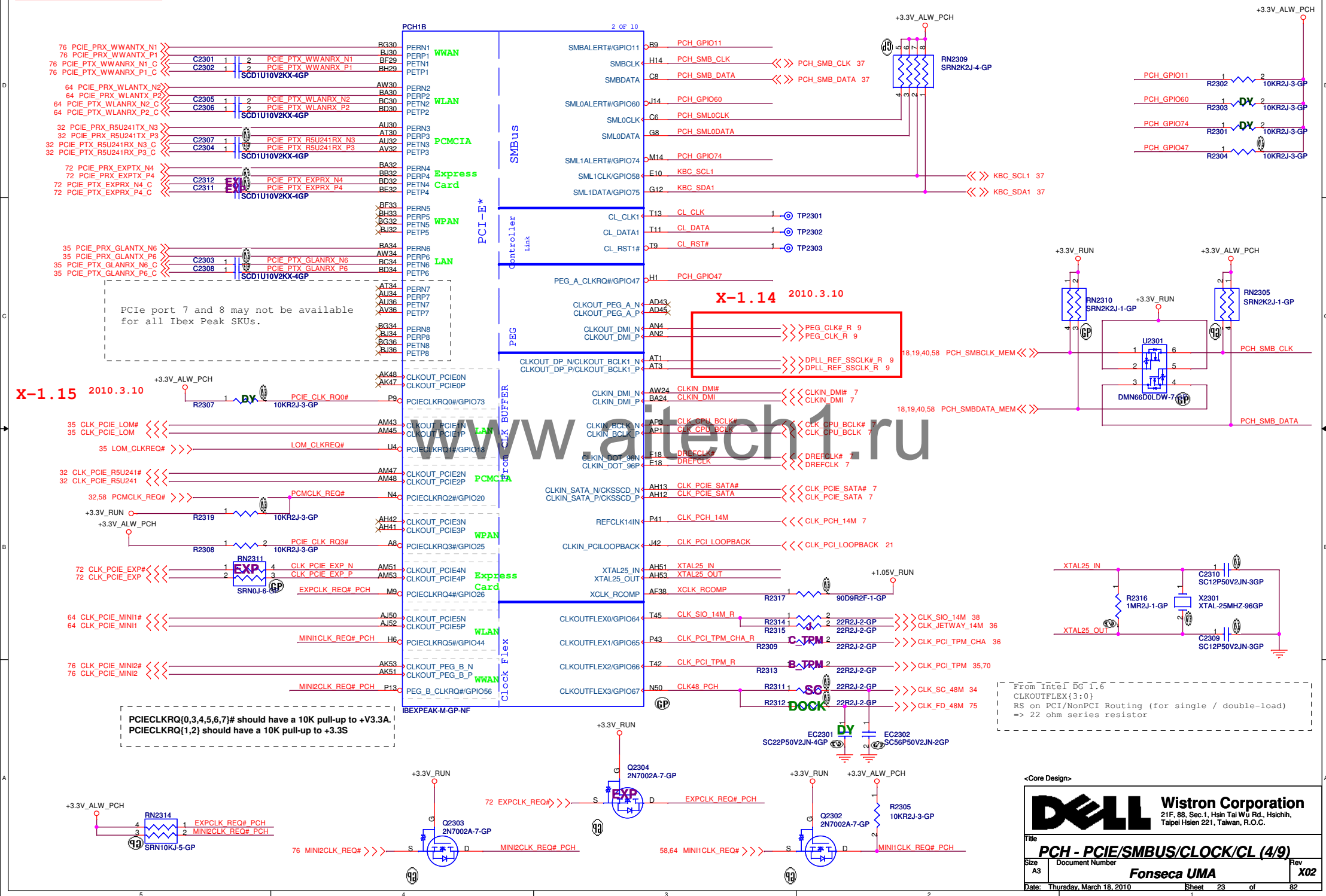
Size: A3 Document Number: **Fonseca UMA** Rev: **X02**

Date: Thursday, March 18, 2010 Sheet: 21 of 82

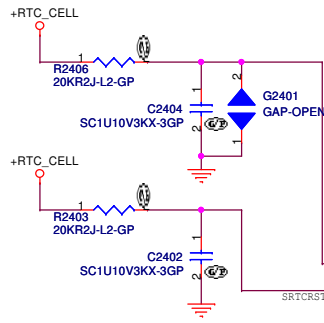
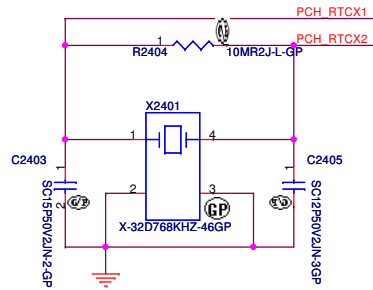
SSID = PCH



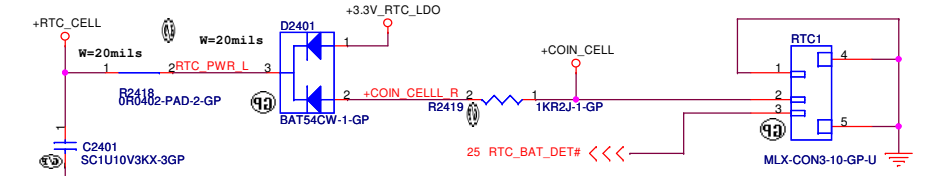
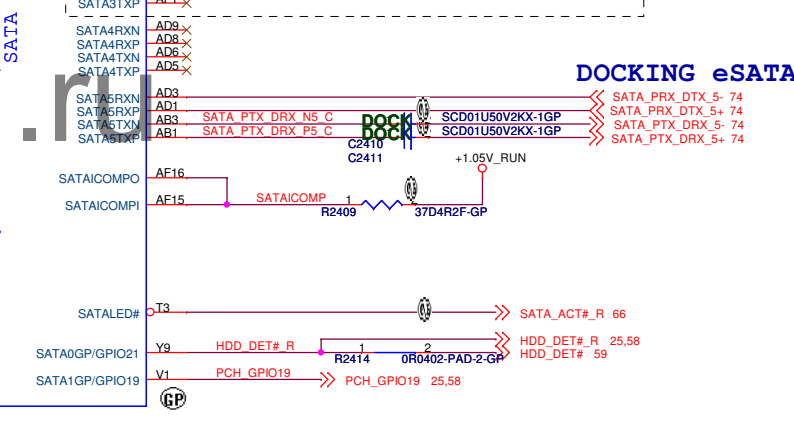
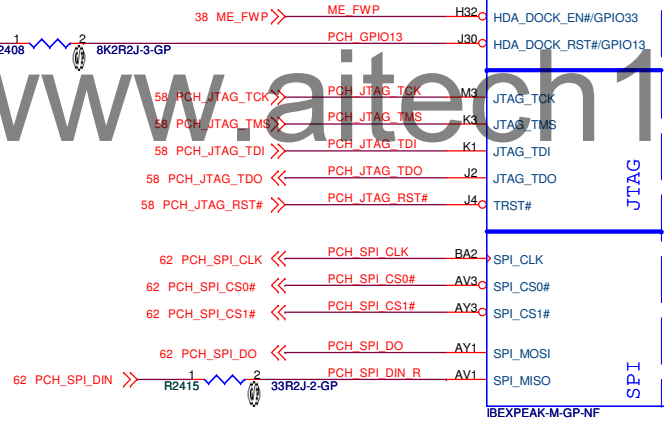
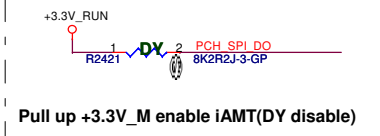
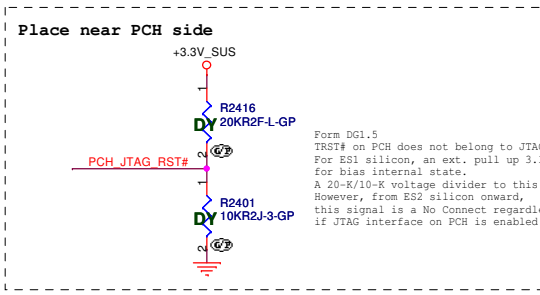
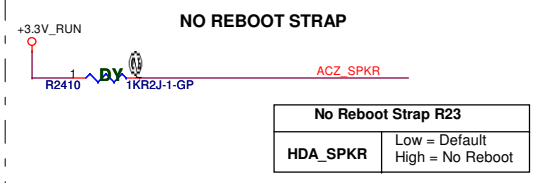
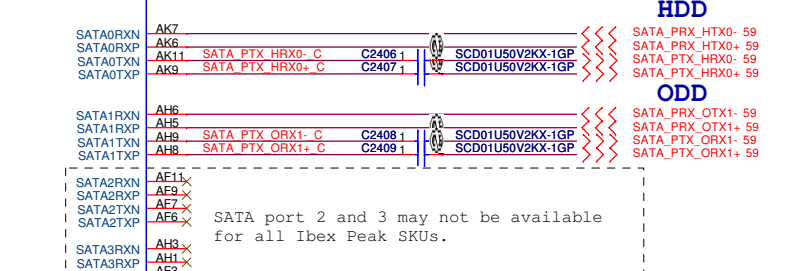
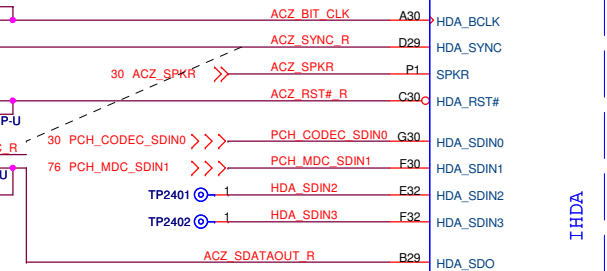
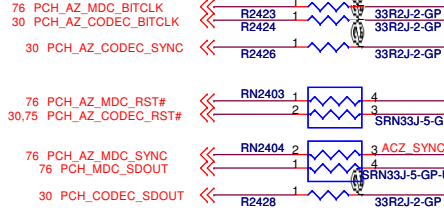
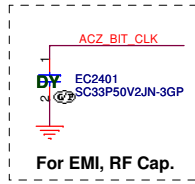
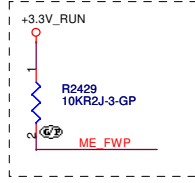
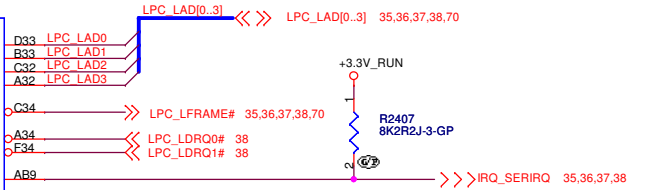
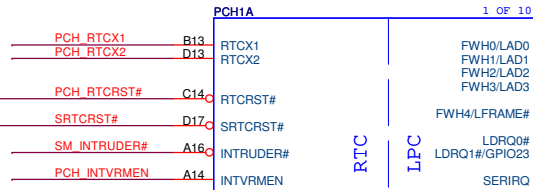
**SSID = PCH**



**SSID = PCH**



INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs



integrated VccSus1_05,VccSus1_5,VccCL1_5	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05	High=Enable	Low=Disable
LAN100_SLP	High=Enable	Low=Disable

20.F1000.003

<Core Design>

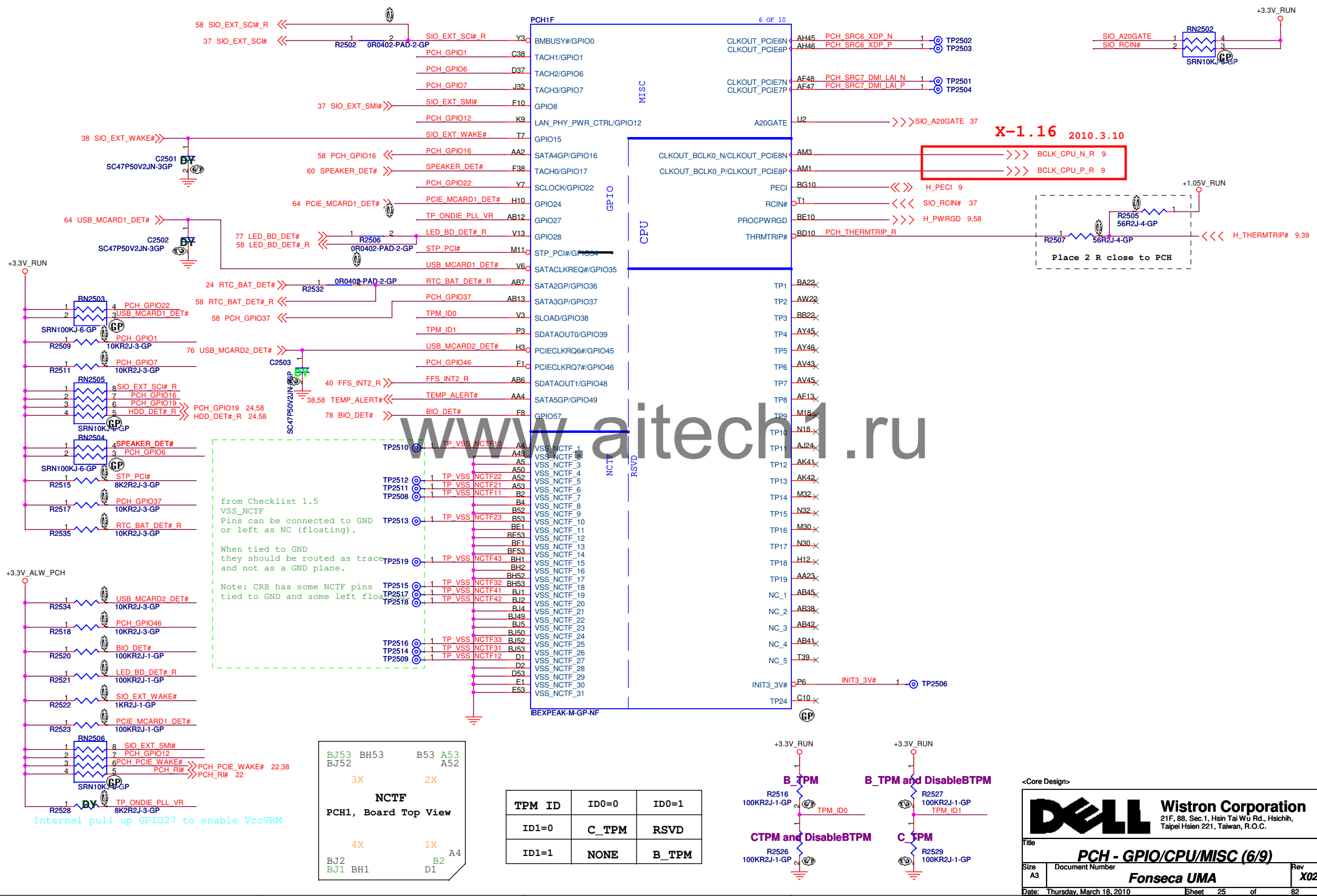
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH - SPI/RTC/LPC/SATA/IHDA (5/9)**

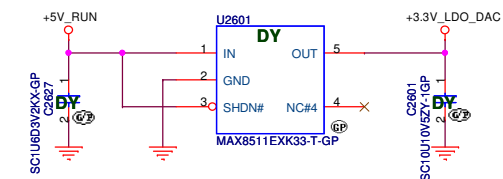
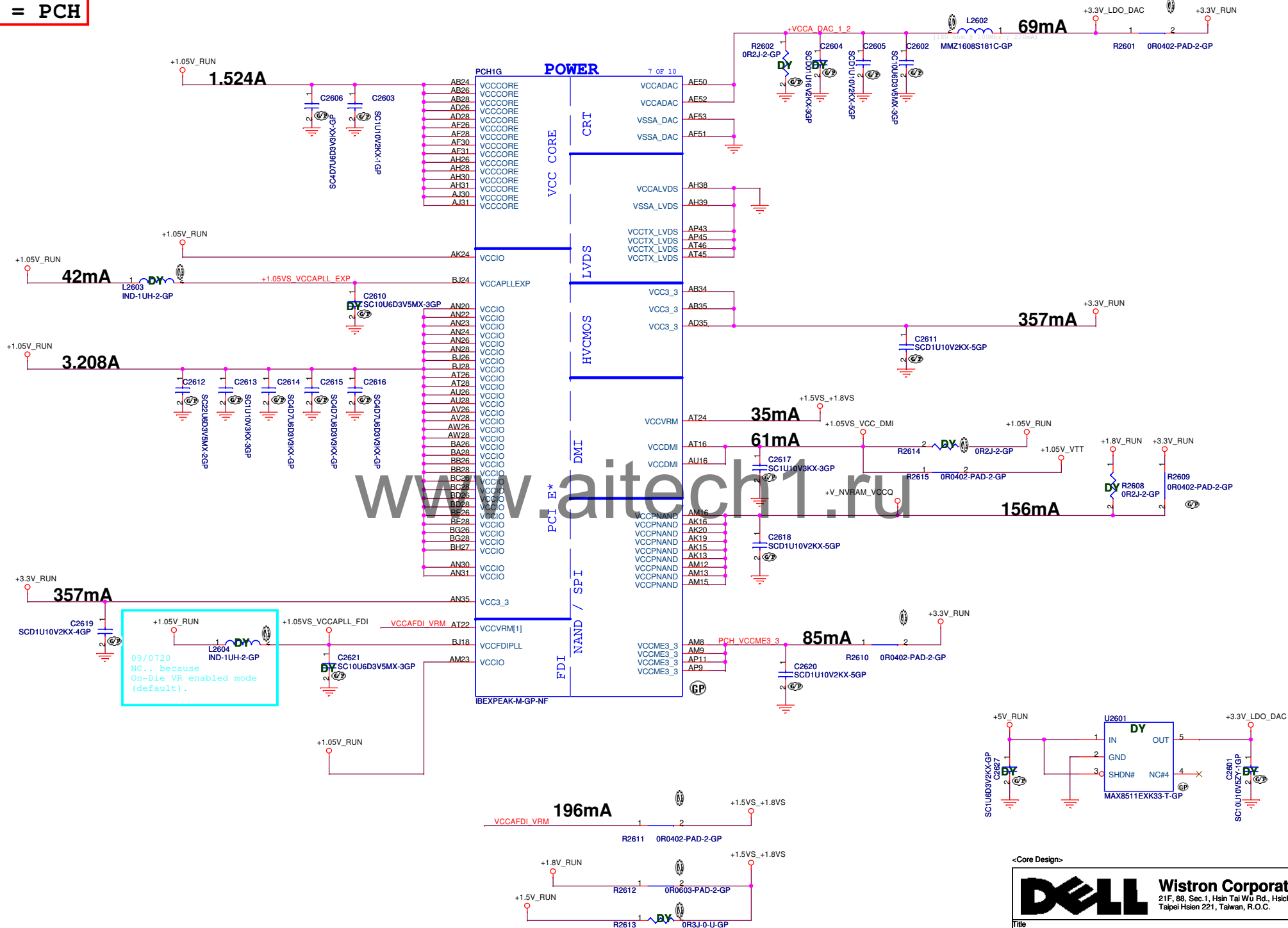
Size: A3 Document Number: **Fonseca UMA** Rev: **X02**

Date: Thursday, March 18, 2010 Sheet: 24 of 82

**SSID = PCH**

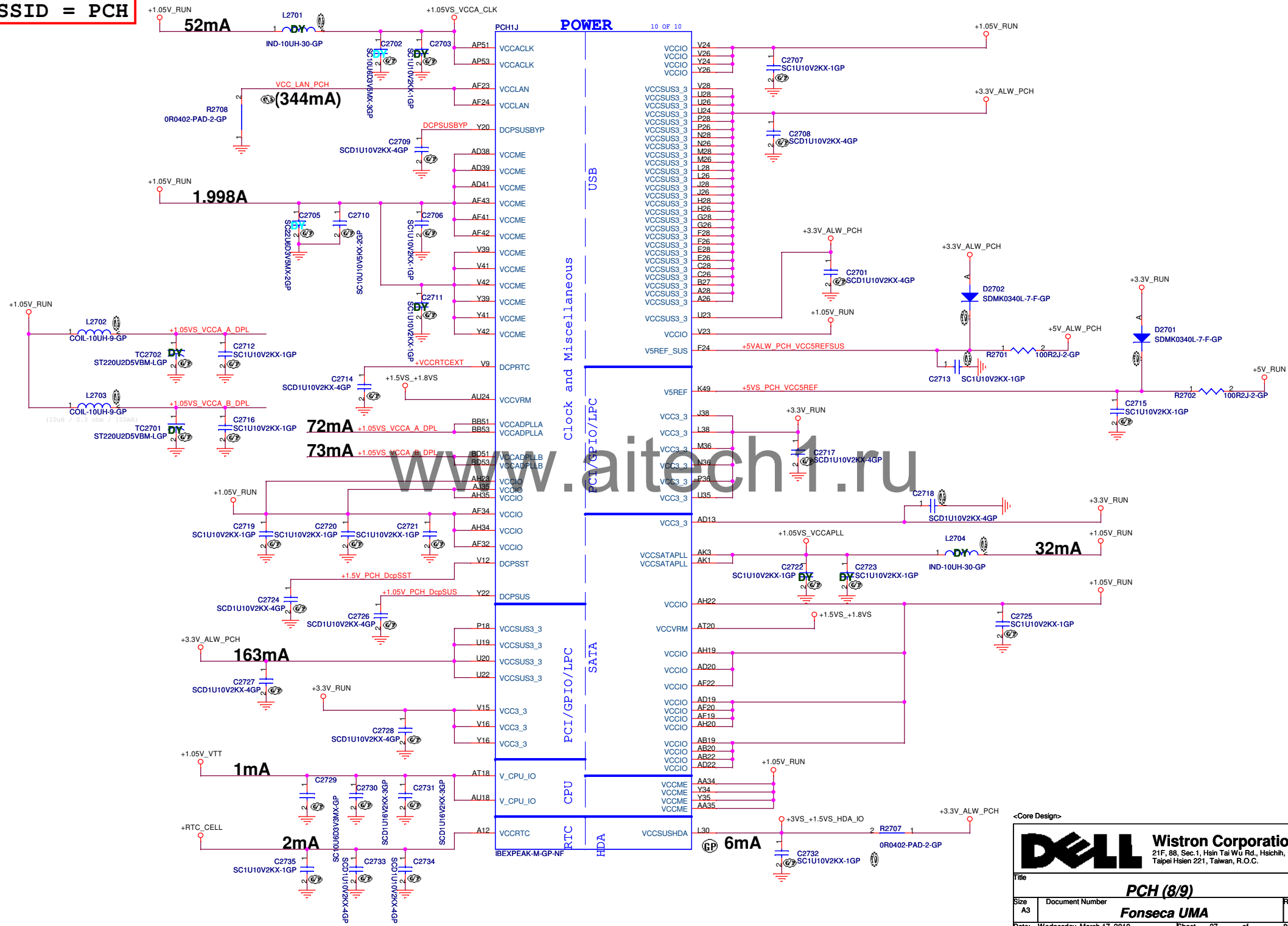


**SSID = PCH**

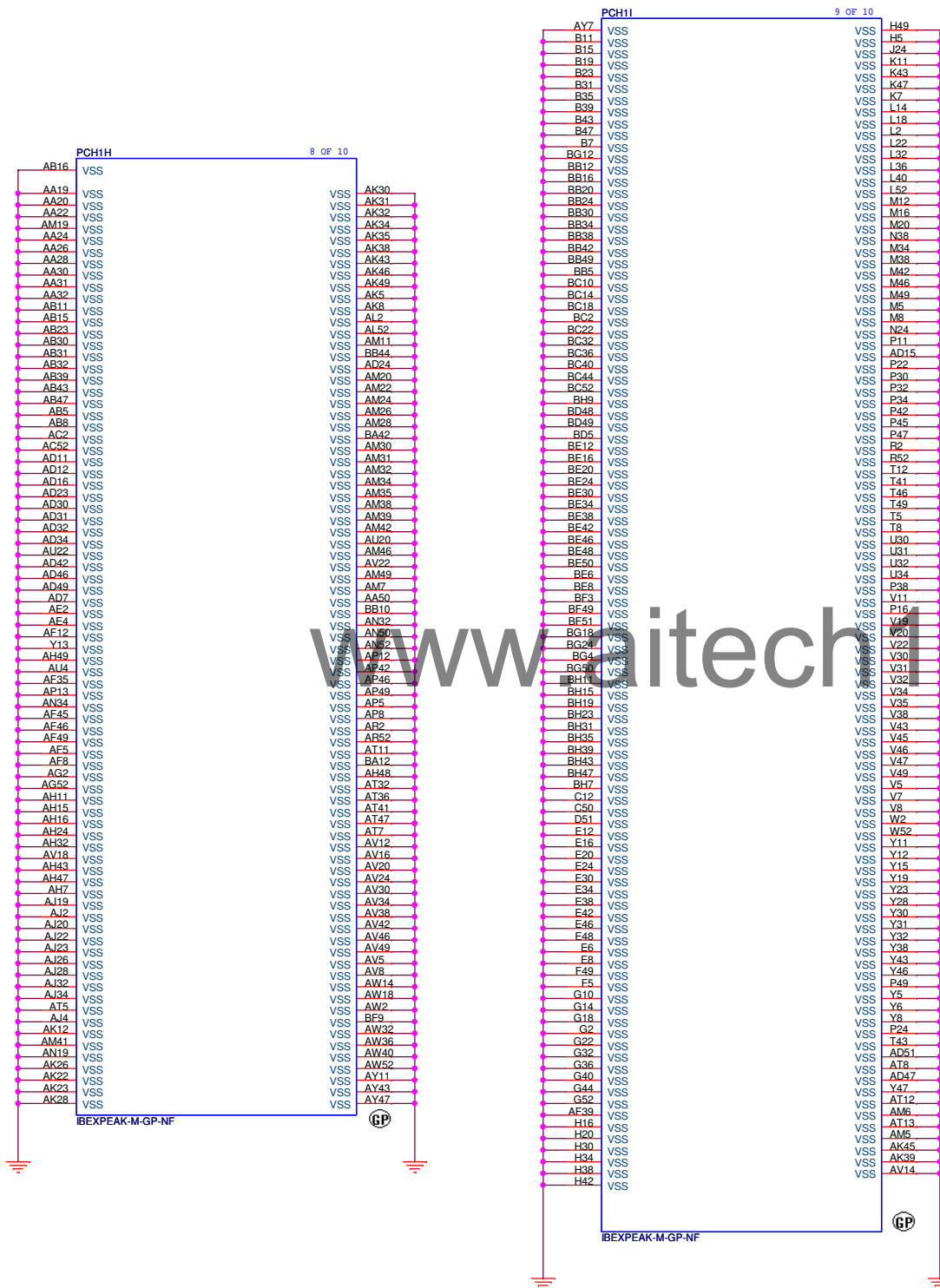




**SSID = PCH**



SSID = PCH






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<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Custom

Document Number

Rev

**Reserve**

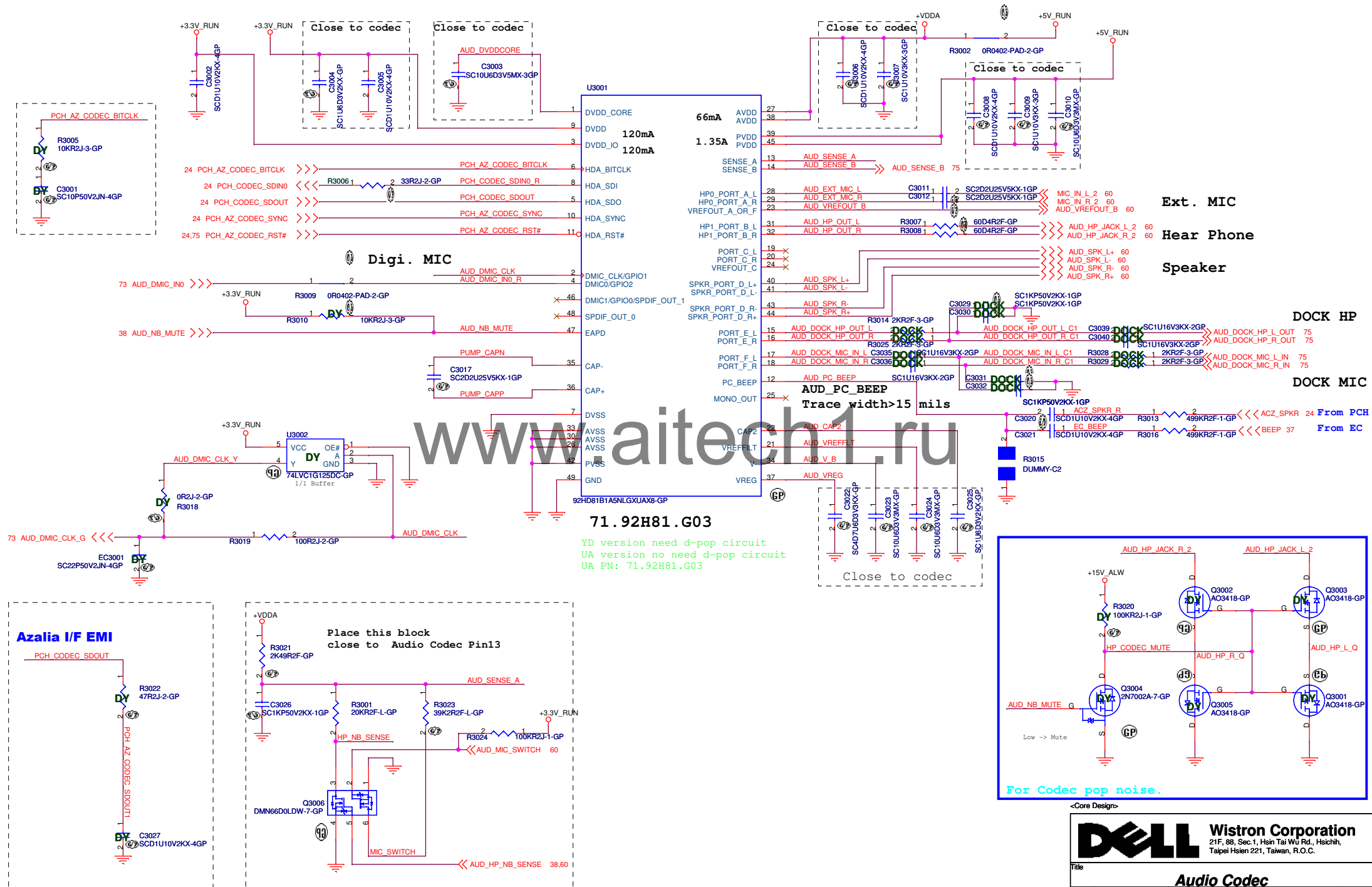
**Fonseca UMA**

**X02**

Date: Wednesday, March 10, 2010

Sheet 29 of 82

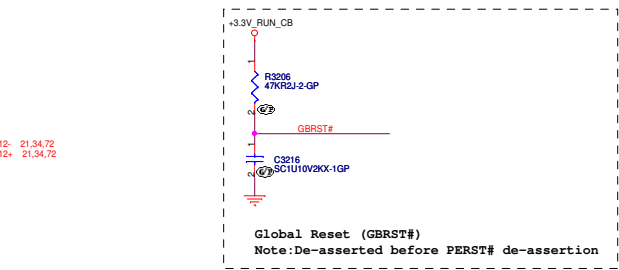
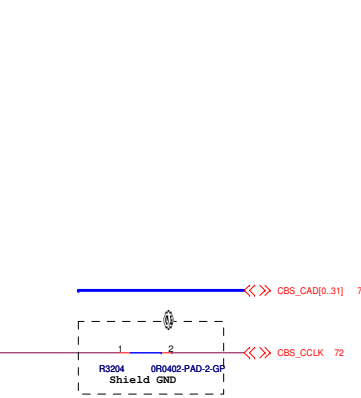
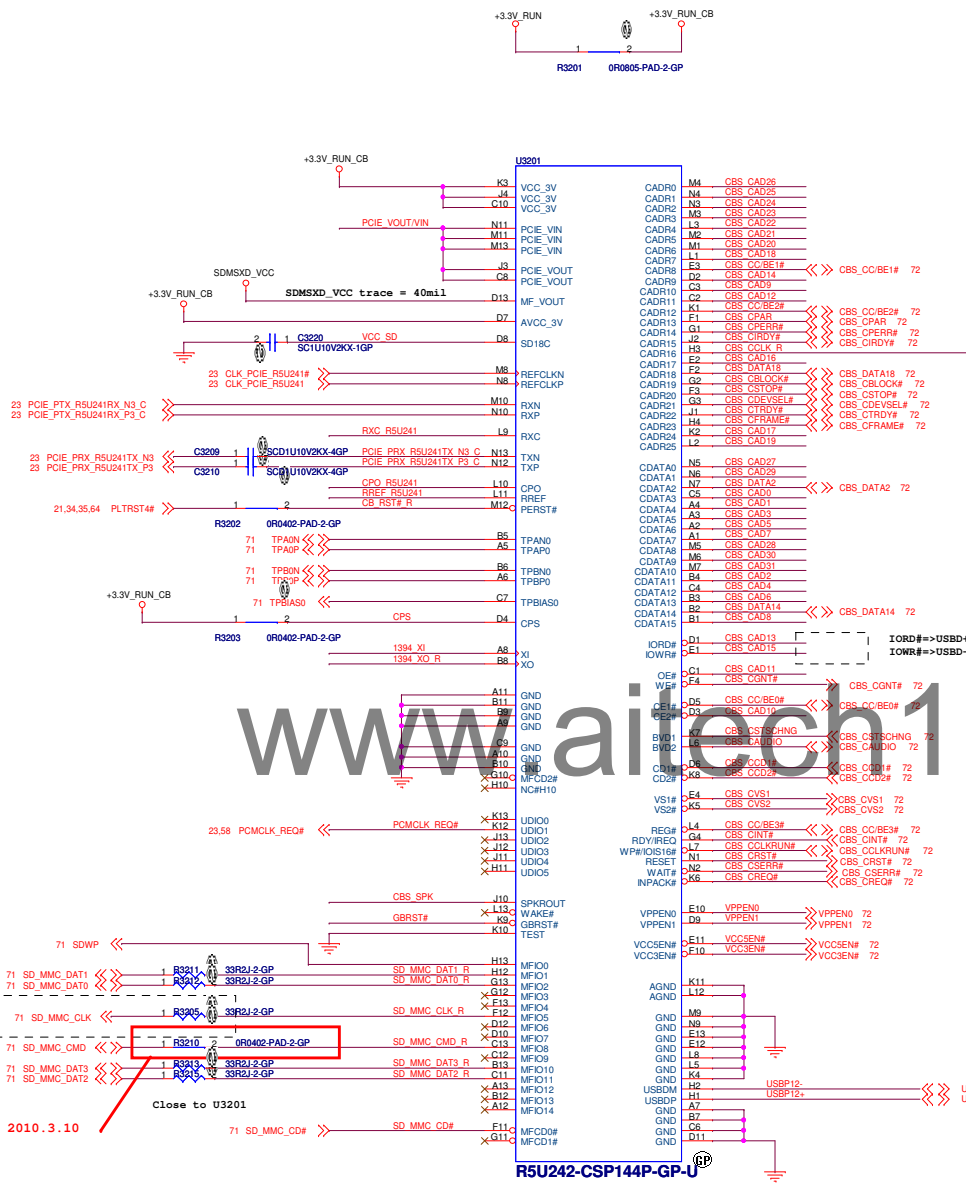
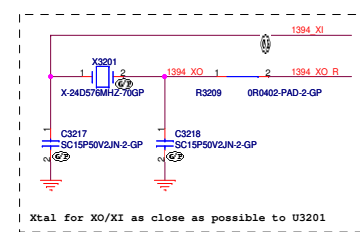
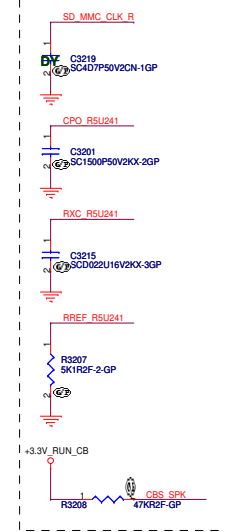
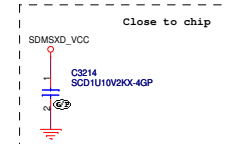
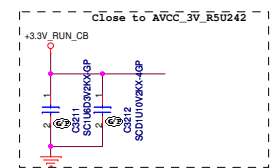
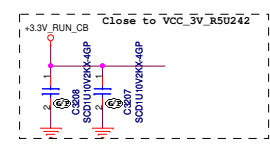
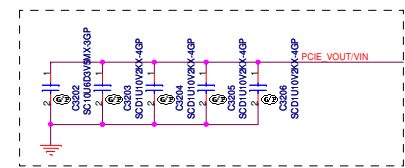
# SSID = AUDIO



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SSID = 1394



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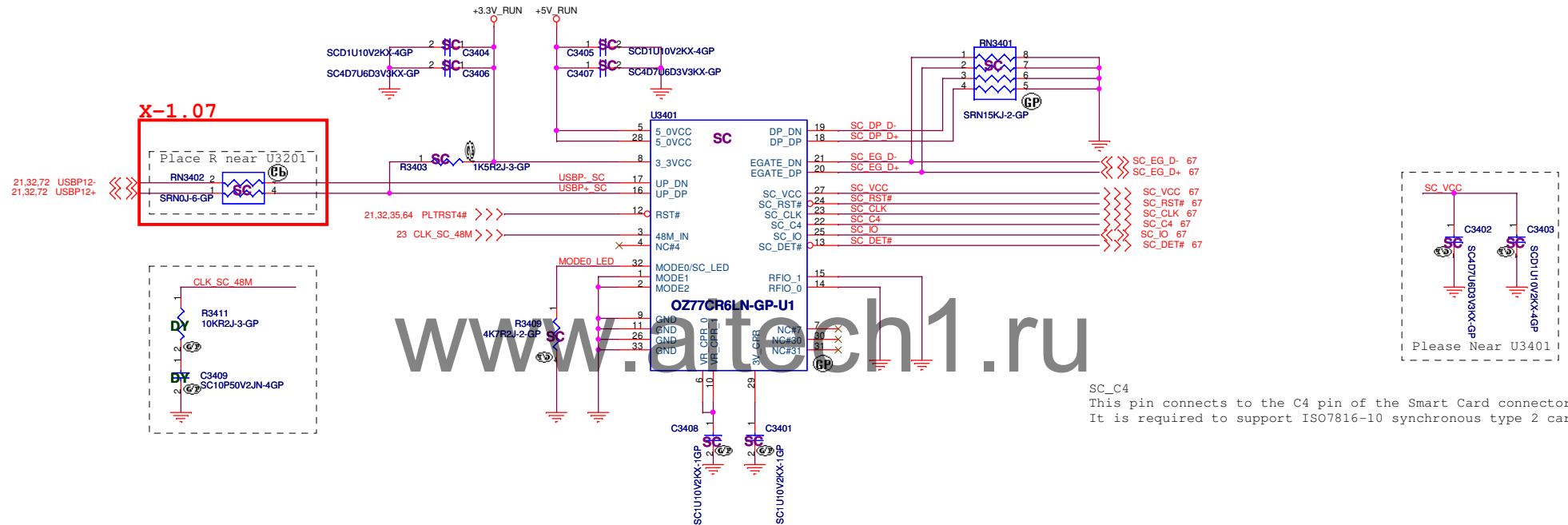
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserve</b>			
Size	Document Number		Rev
Custom	<b>Fonseca UMA</b>		<b>X02</b>
Date:	Wednesday, March 10, 2010		Sheet 33 of 82

SSID = SmartCard

## SmartCard Chip

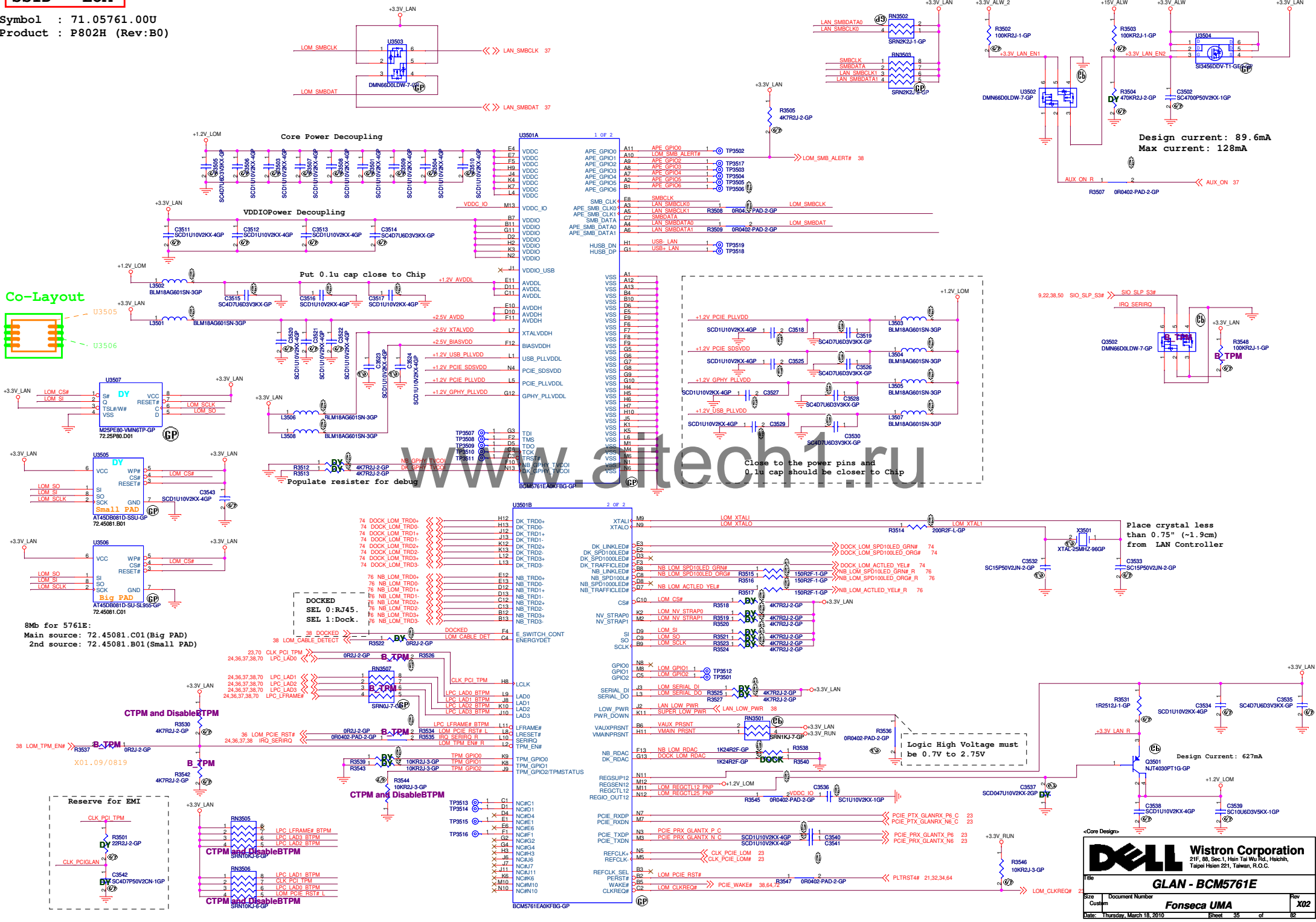


SC\_C4  
This pin connects to the C4 pin of the Smart Card connector.  
It is required to support ISO7816-10 synchronous type 2 cards.

MODE0 / SC_LED	<p>This terminal is an output indicating Smart Card activity; capable to drive an external LED device.</p> <p>The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit.</p> <p>When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1).</p> <p>When sampled low (4.7k), the downstream port device is removable.</p> <p>When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.</p>
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device.
RFIO_1	If contactless is disabled, then this terminal shall be pulled-down to GND through a pull-down resistor, or directly connected to GND.

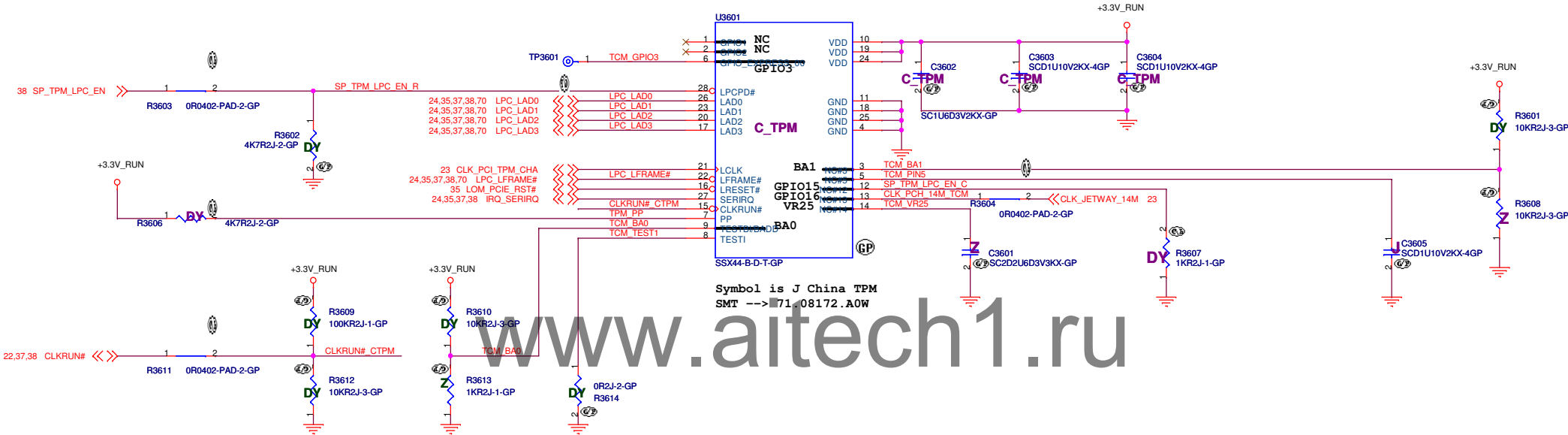
Symbol : 71.05761.00U  
Product : P802H (Rev:B0)



# SSID = TCM

Symbol : Jetway, but linked to ZTE  
 Product : 71.08172.00W (ZTE)

## China TPM Chip



Symbol is J China TPM  
 SMT --> 71.08172.A0W

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

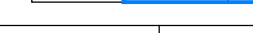
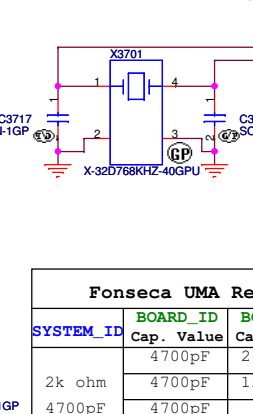
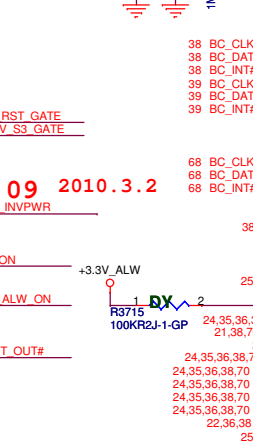
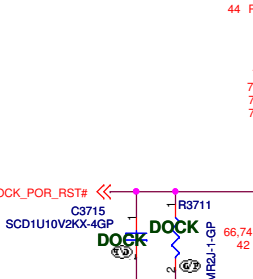
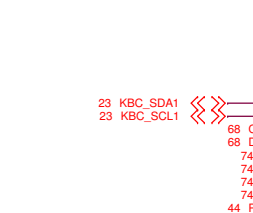
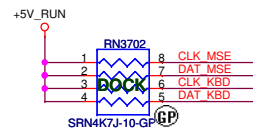
Default EE/EF as Any recommended

PIN12	FLASH	SRAM
1(default)	0	

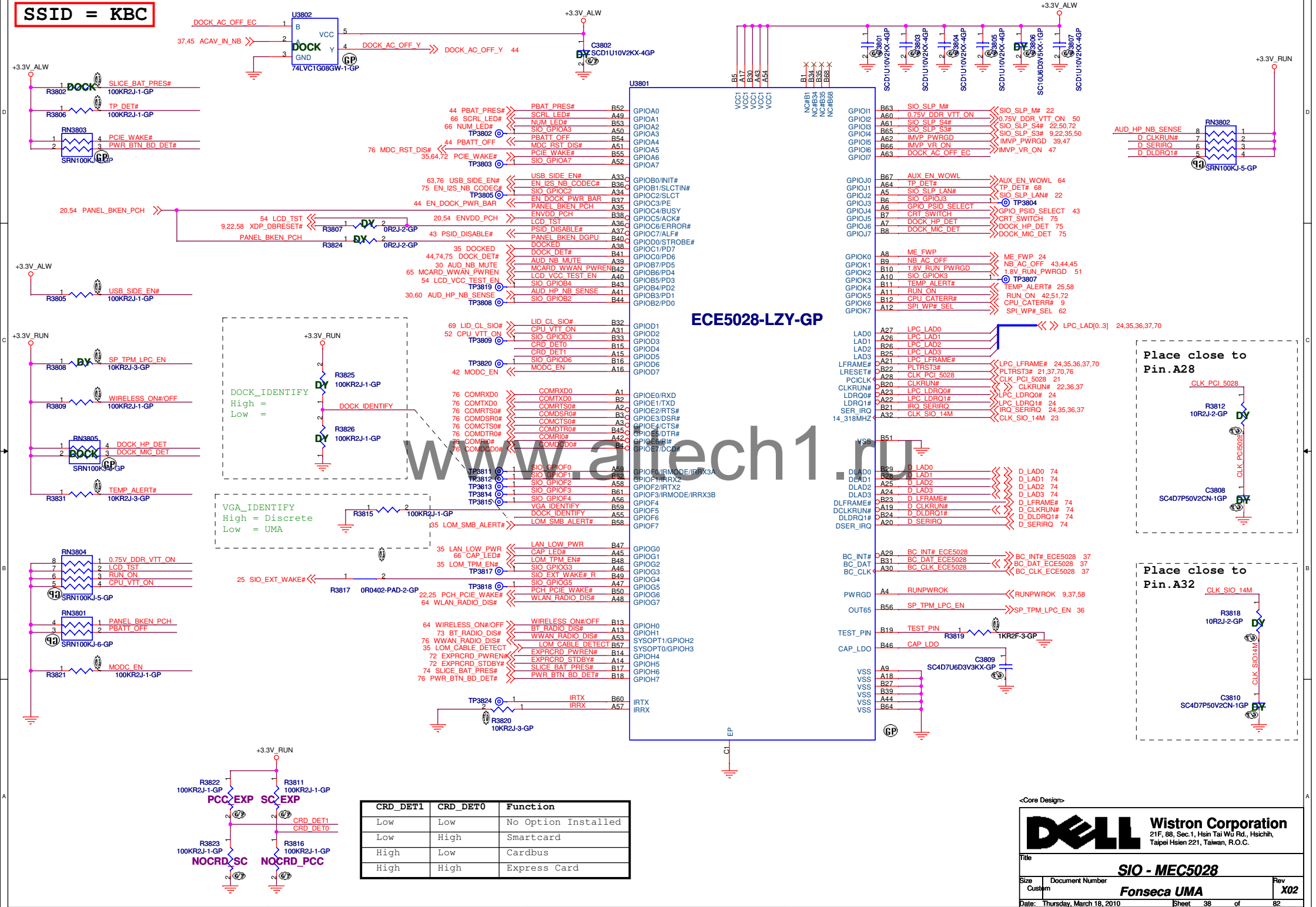
J has internal PU with PIN12.



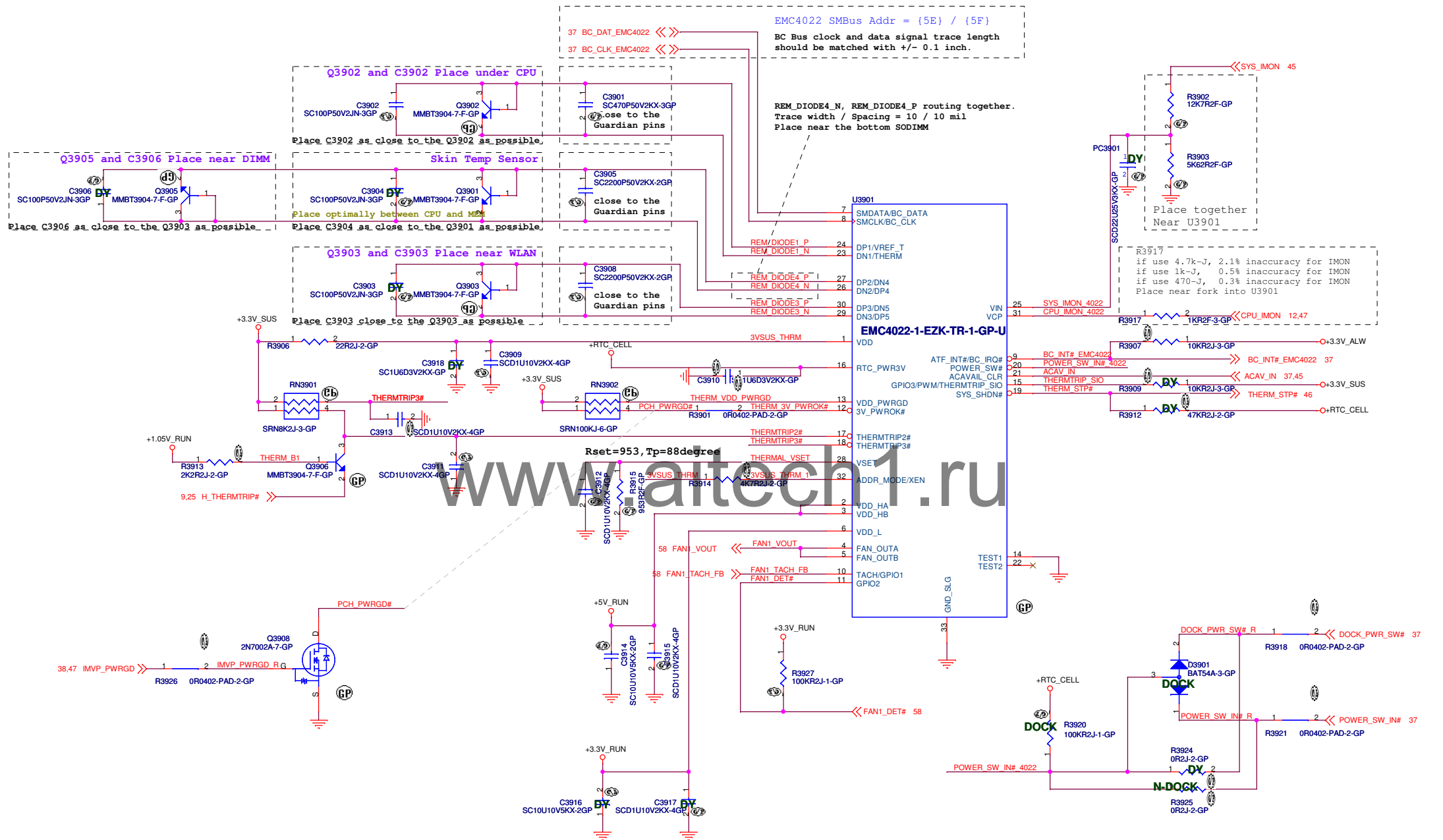
SSID = KBC



**SSID = KBC**



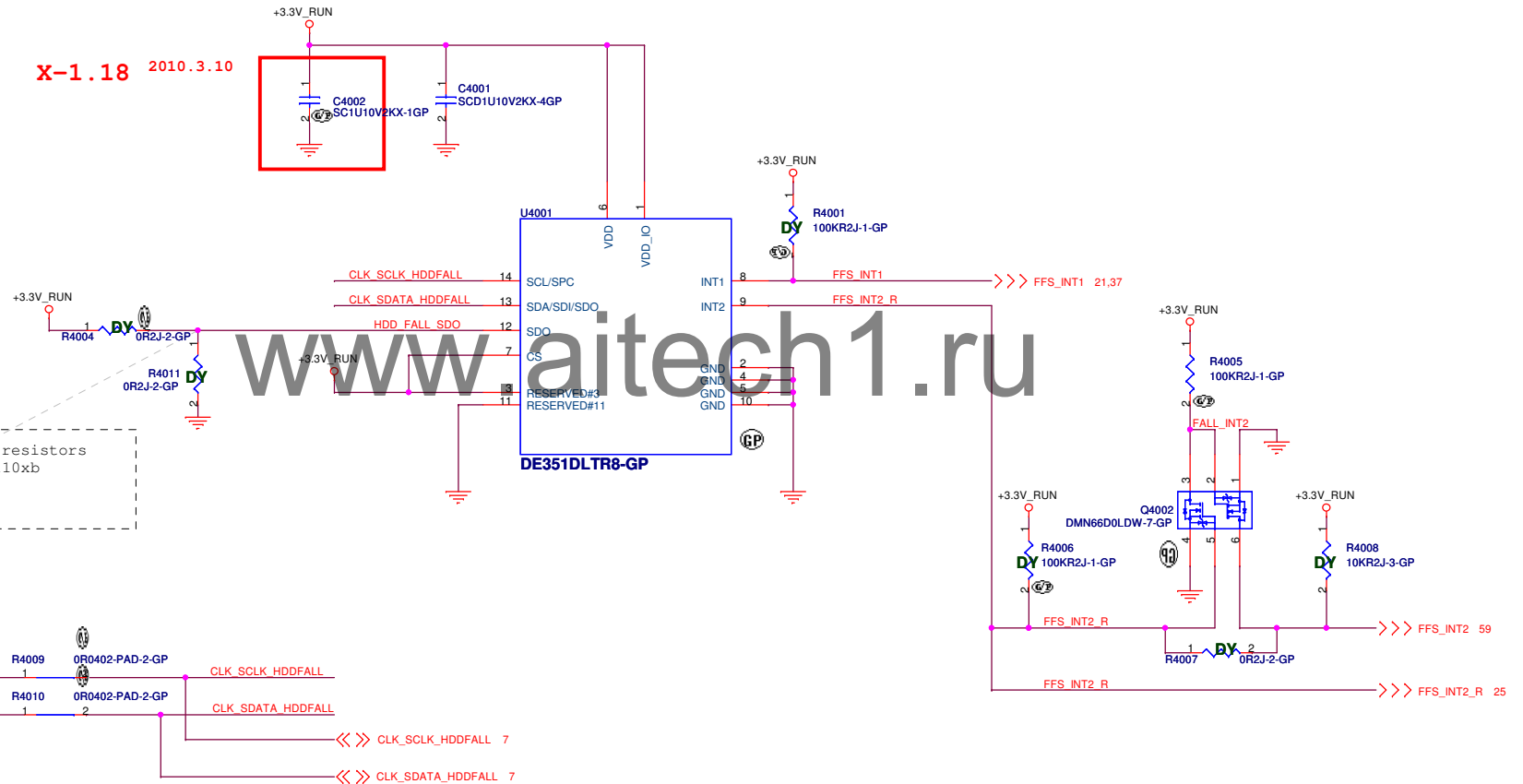
# SSID = Thermal



<Core Design>

<b>DELL</b>			<b>Wistron Corporation</b>		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title <b>Thermal, Fan controller</b>					
Size Custom	Document Number <b>Fonseca UMA</b>				Rev <b>X02</b>
Date: Thursday, March 18, 2010		Sheet 39		of 82	


# Free Fall Sensor



SSID = Reset.Suspend

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<Core Design>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

*Power On Logic*

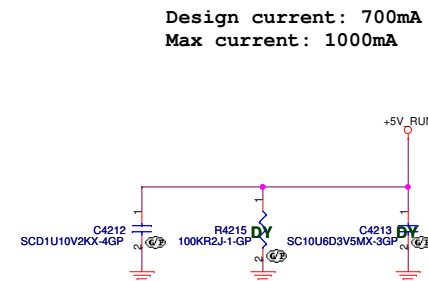
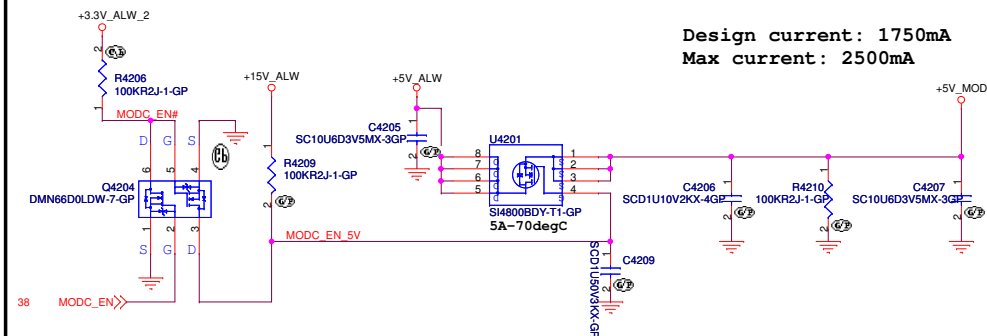
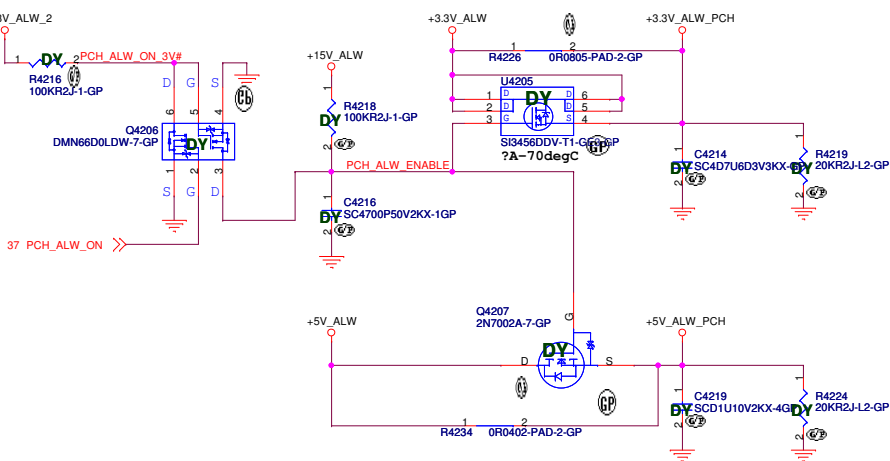
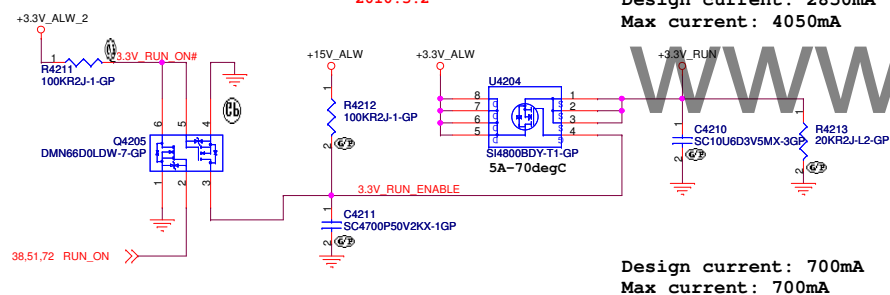
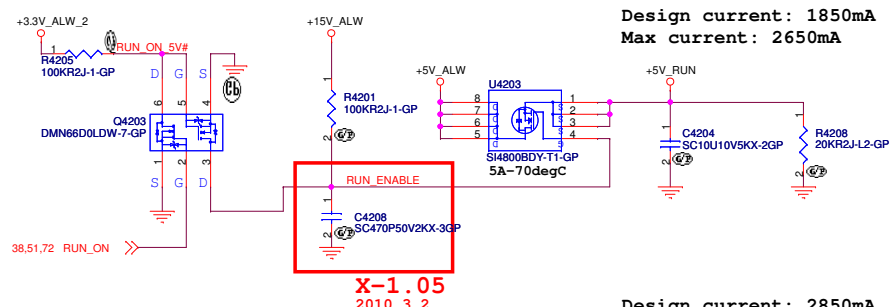
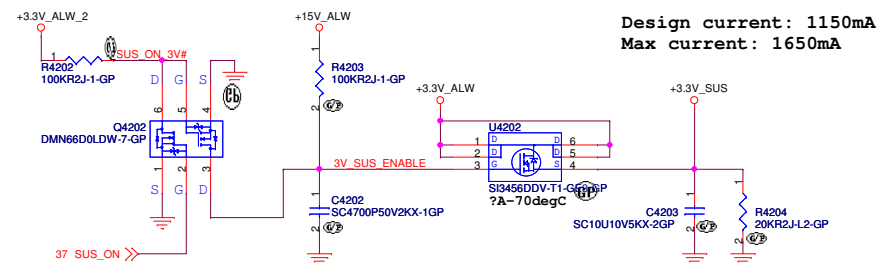
Size  
A3

Document Number  
*Fonseca UMA*

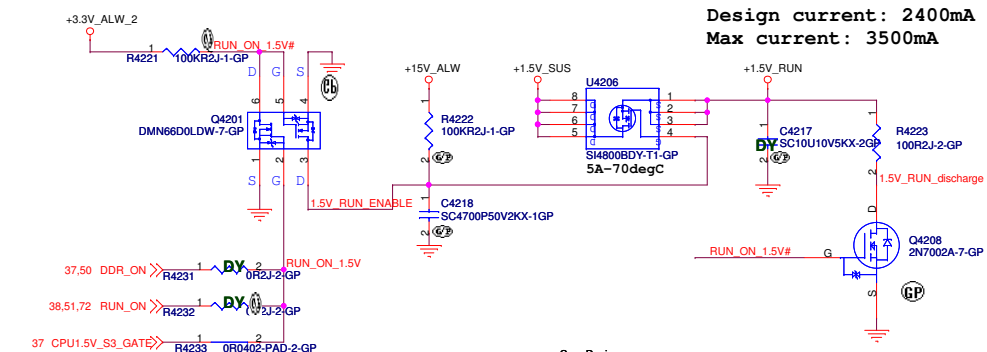
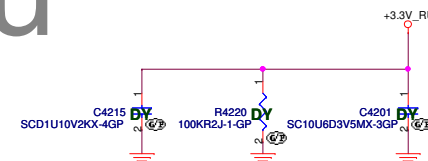
Rev  
*X02*

Date: Wednesday, March 10, 2010Sheet 41 of 82

# SSID = Reset .Suspend



place to HDD connector side



<Core Design>



Title			Power Plane Enable
Size	Document Number	Rev	X02
Custom	Fonseca UMA		
Date: Wednesday, March 17, 2010	Sheet	42	of 82

SSID = PWR.Support

Adapter In

\*PIN NAME DIFFERENCES\*

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

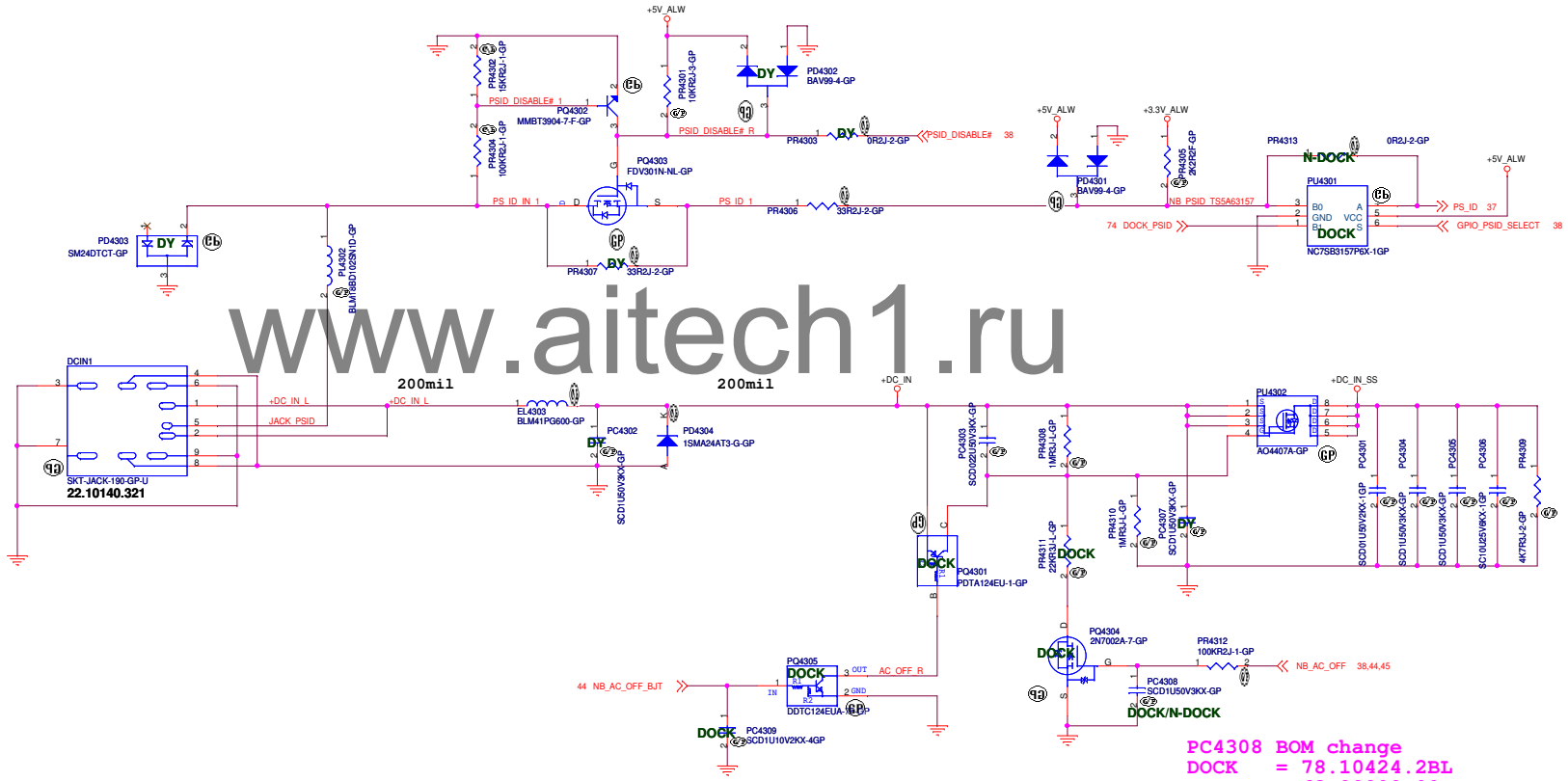
"NC" means no-connect

DC IN CONN

PIN 3,4	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

TABLE  
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	10K 1%
R412	DUMMY	DUMMY	10K 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	DUMMY	10K 5%
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%



PC4308 BOM change  
DOCK = 78.10424.2BL  
N-DOCK = 63.00000.00L

MAX 8731A/ISL88731

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

\*R504 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adapter.

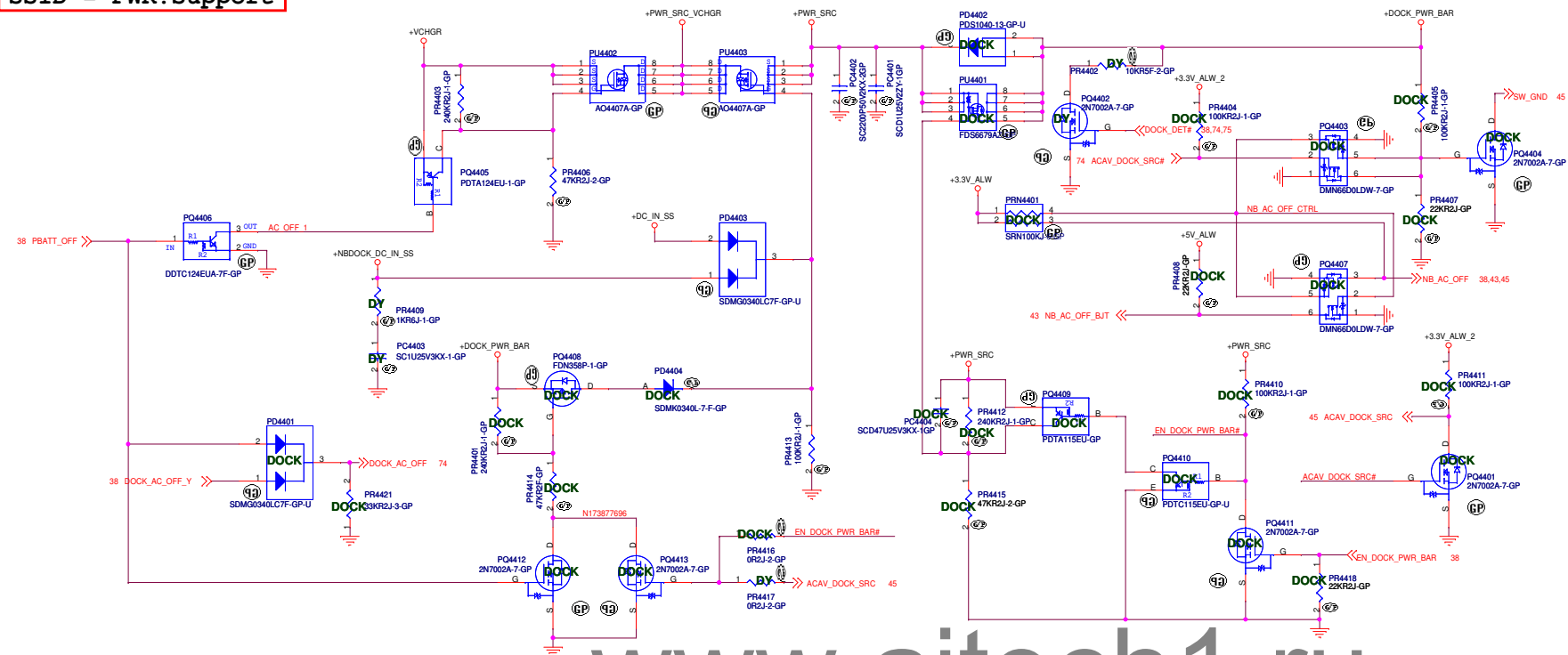
BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

\*R504 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adapter.

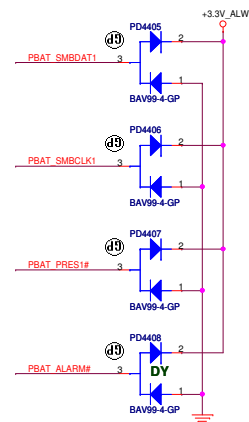
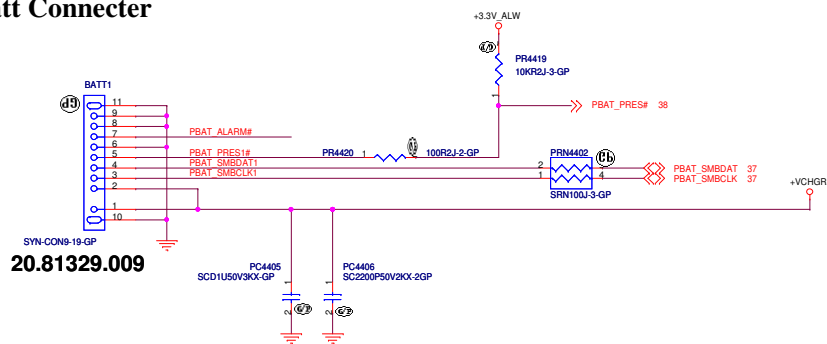


```
SSID = PWR.Support
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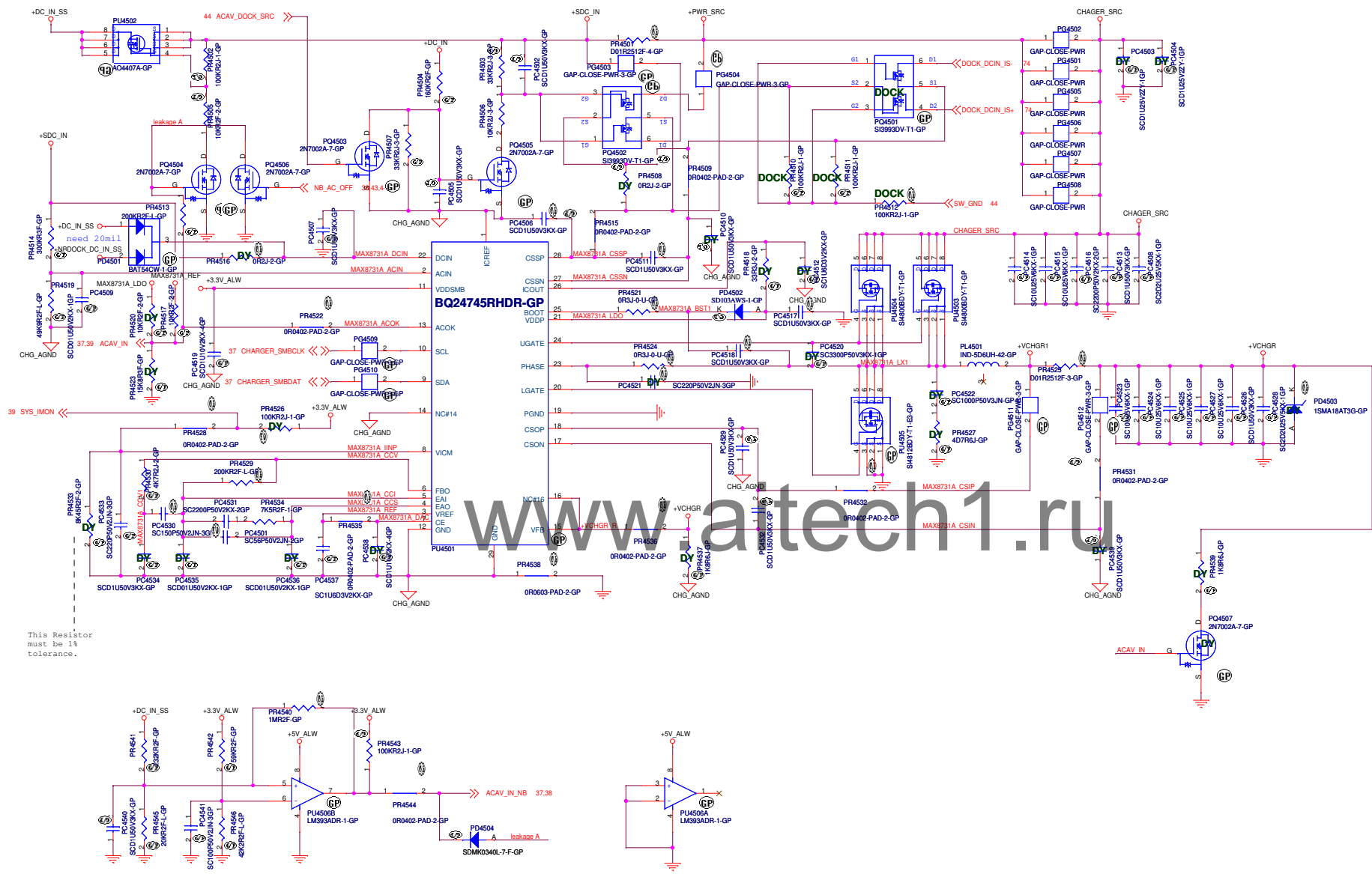


## SSID = RBATT

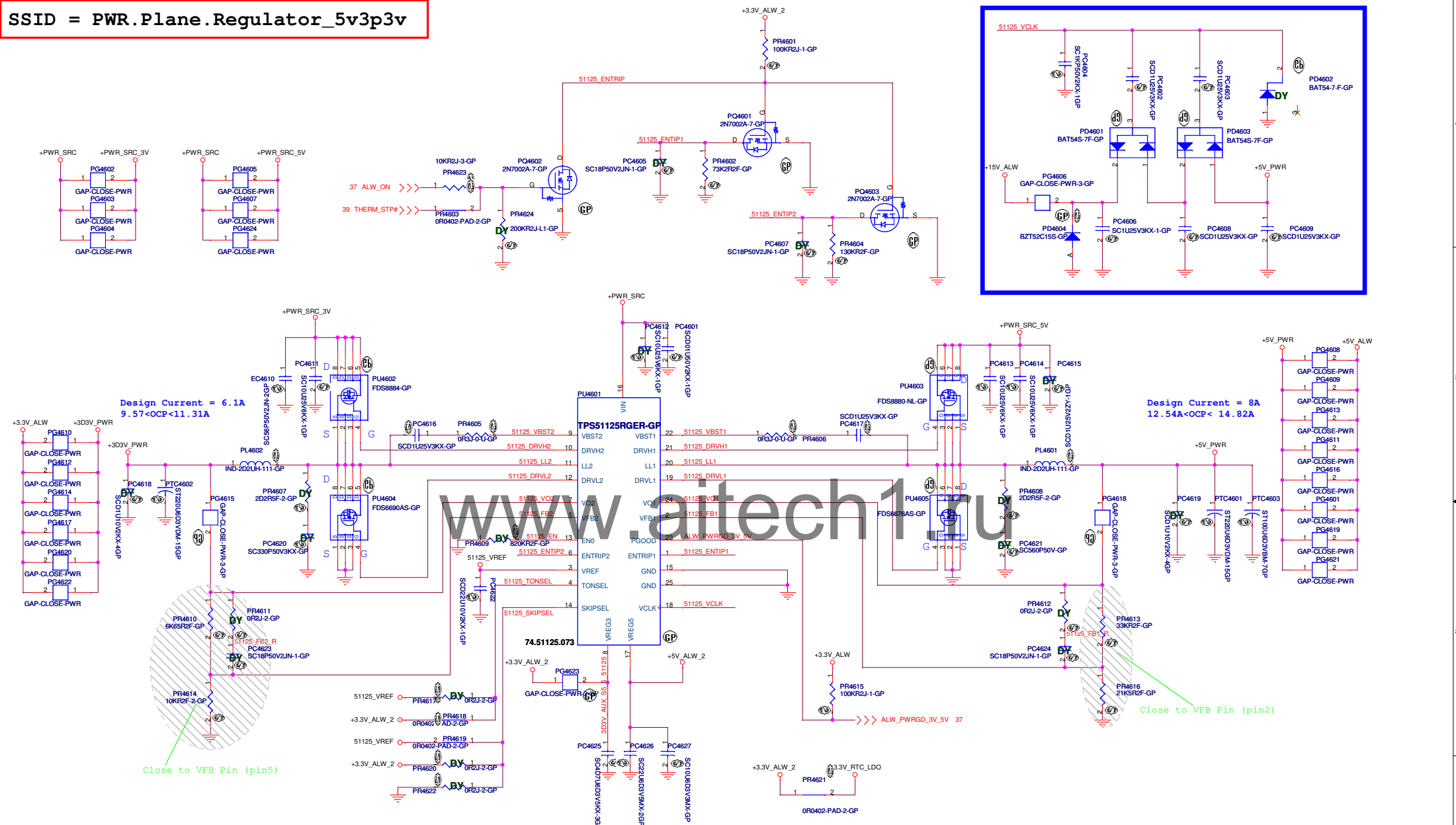
## Batt Connector



# SSID = Charger



SSID = PWR.Plane.Regulator\_5v3p3v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: FDVE0630-1R5M=P3 TOKO 10.6 mohm Isat =10.7Arms 68.1R510.10Y  
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC\_TOKIN/77.C2271.00L  
 O/P cap: 100U 6.3V 6TPE100MAZB 35mOhm 1.4Arms SANYO/77.21071.07L  
 H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037  
 L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: FDVE0630-2R2M=P3 TOKO 14mohm Isat =9.4Arms 68.2R21B.10A  
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC\_TOKIN/77.C2271.00L  
 H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037  
 L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

<Core Design>

**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **DCDC 5V/3D3V (TPS51125)**

Size: Custom Document Number

Customer: **Fonseca UMA**

Date: Wednesday, March 17, 2010

Sheet: 46 of 82


Rev: X02



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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserve

Size A3	Document Number Fonseca UMA	Rev X02
Date: Wednesday, March 10, 2010		Sheet 48 of 82

SSID = PWR.Plane.Regulator\_1p05v

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

DC to DC 1.05V

Size  
A3

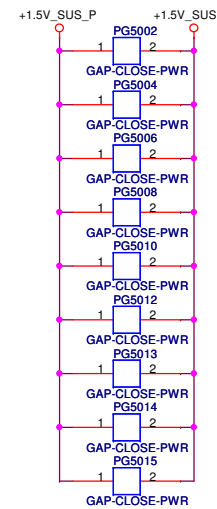
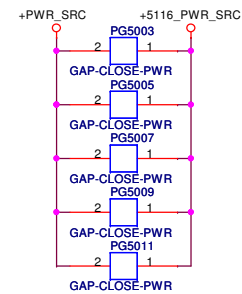
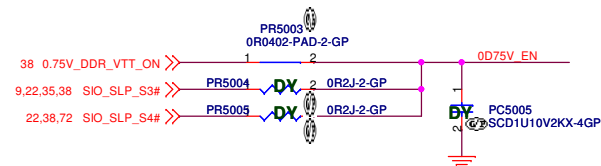
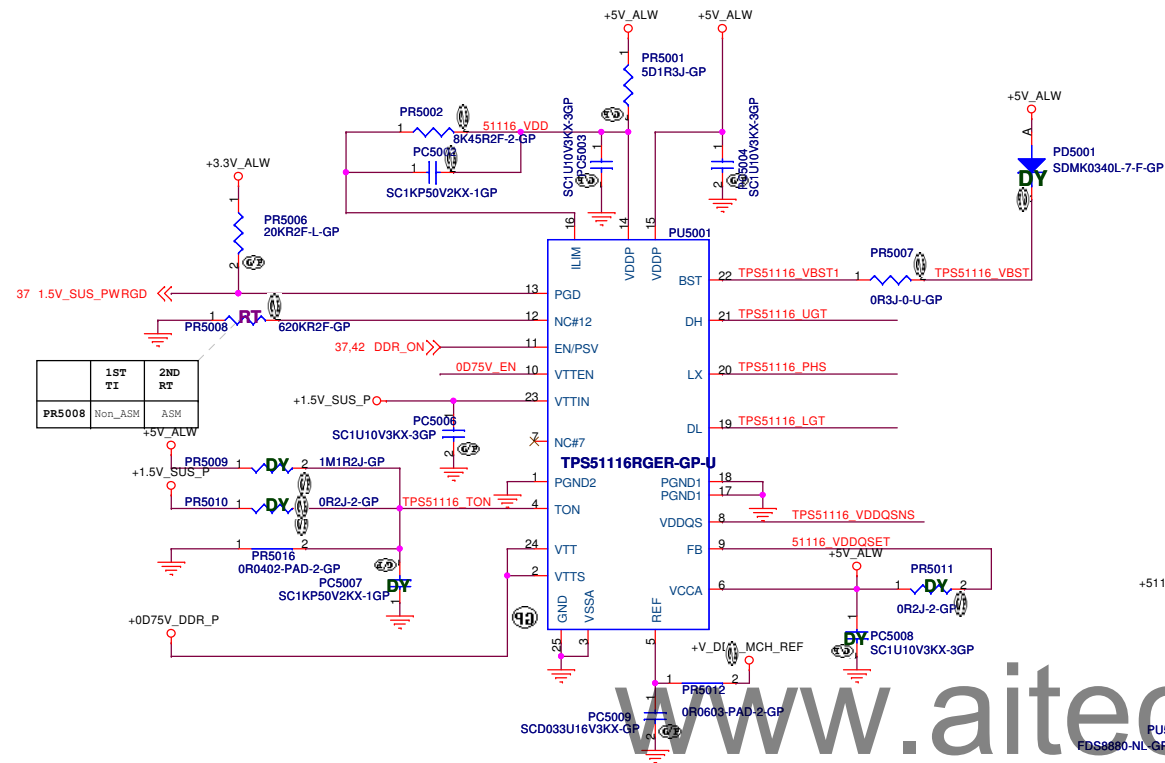
Document Number  
Fonseca UMA

Rev  
X02

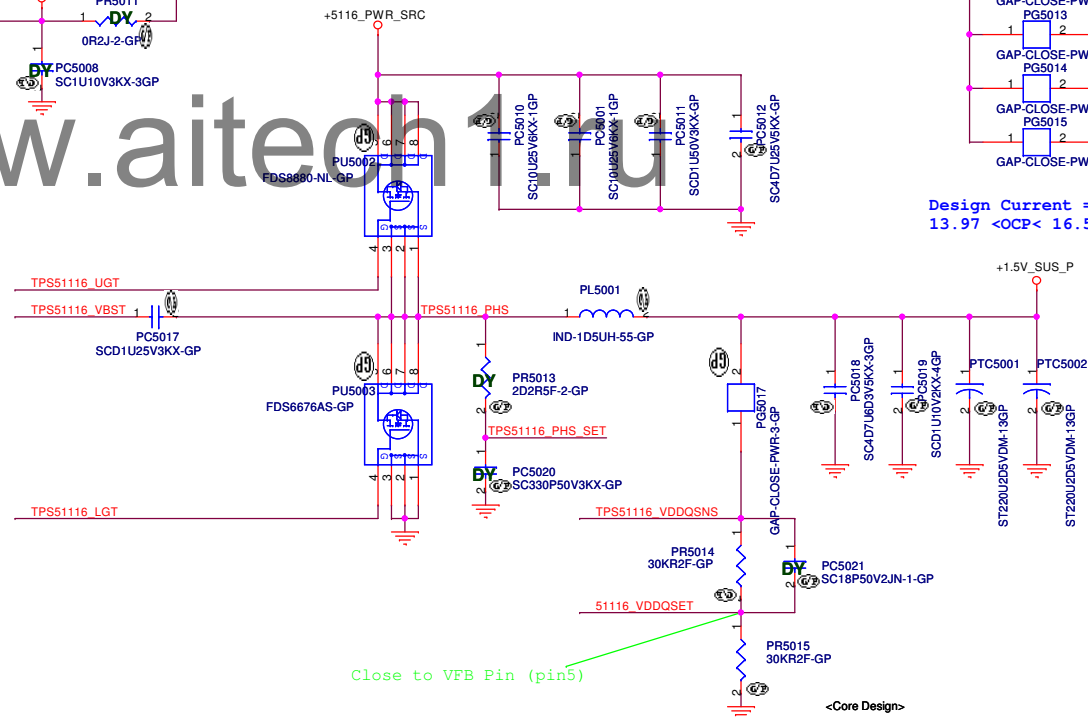
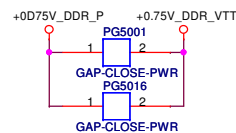
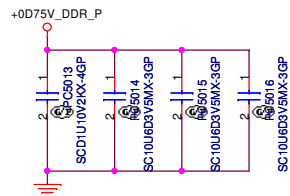
Date: Wednesday, March 10, 2010

Sheet 49 of 82

SSID = PWR.Plane.Regulator\_1p5v0p75v



Design Current = 8.9A  
13.97 <OCV< 16.51A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: FDU1040-1R5M=P3 TOKO DCR:3.86 mohm Isat =19.7Arms 68.1R510.10Q  
O/P cap: TLP5LV0G227M(25)12RE 25mOhm 2.5Arms NEC\_TOKIN/ 77.C2271.07L  
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037  
L/S: FDS8672S SO-8/ 5.3mohm/7.0mohm@4.5Vgs/ 84.08672.A37  
Switching freq-->400KHz

<Core Design>

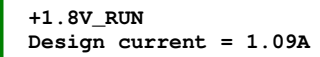
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File **DC to DC 1.5V / 0.75V**

Size	Document Number	Rev
Custom	<b>Fonseca UMA</b>	<b>X02</b>
Date:	Wednesday, March 17, 2010	Sheet 50 of 82



### ***LDO for +1.8V\_RUN***



SSID = PWR.Plane.Regulator\_1p05v

## TPS51218 for +1.05V\_VTT

Frequency setting  
420K -->290KHz  
200K -->340KHz  
100K -->380KHz  
39K -->430KHz

$$V_{out} = 0.704V * (R1 + R2) / R2$$

Max. Current = 18A  
Design Current = 18A  
19.8<OCP<23.4A

<Core Design>

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **DC to DC +1.05V\_VTT**  
Size Document Number **Fonseca UMA** Rev **X02**  
Date: Wednesday, March 17, 2010 Sheet 52 of 82

```
SSID = CPU.GFX.Regulator
```



Max. Current = 22A  
Design Current = 15.4A  
24.2A < OCP < 28.6A



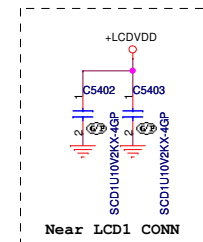
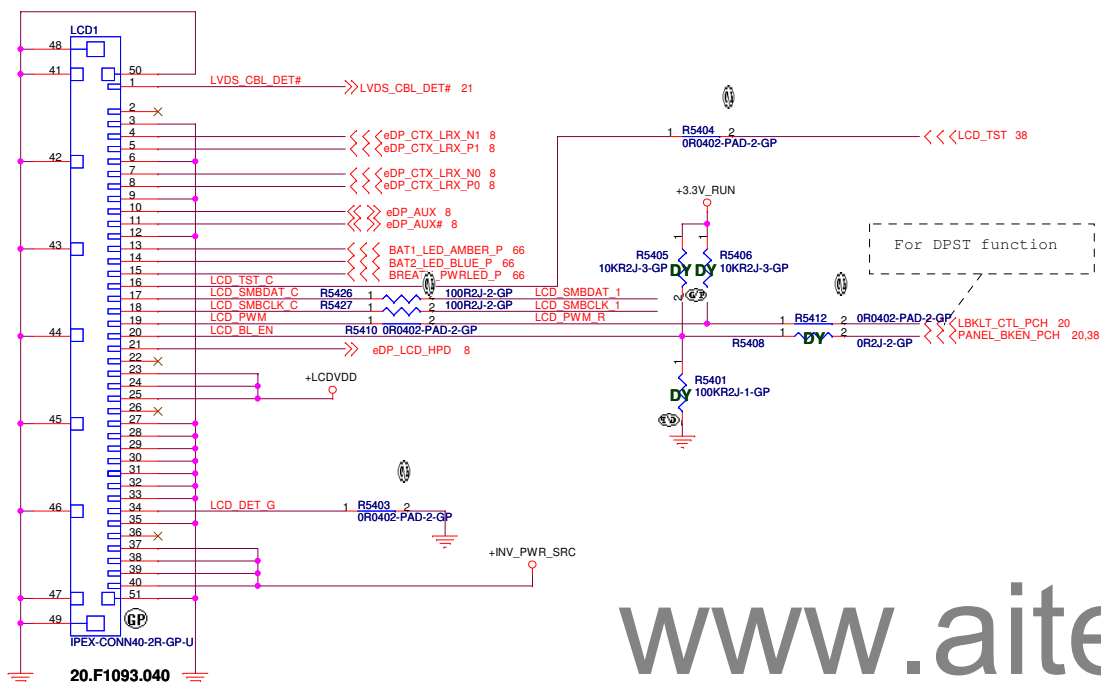
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>ADP3211 CPU GFXCORE</b>			
Size	Document Number	Rev	
Custom	<b>Fonseca UMA</b>		<b>X02</b>
Date:	Wednesday, March 17, 2010	Sheet	53 of 82

SSID = VIDEO

LED Location from left to right

BATTERY



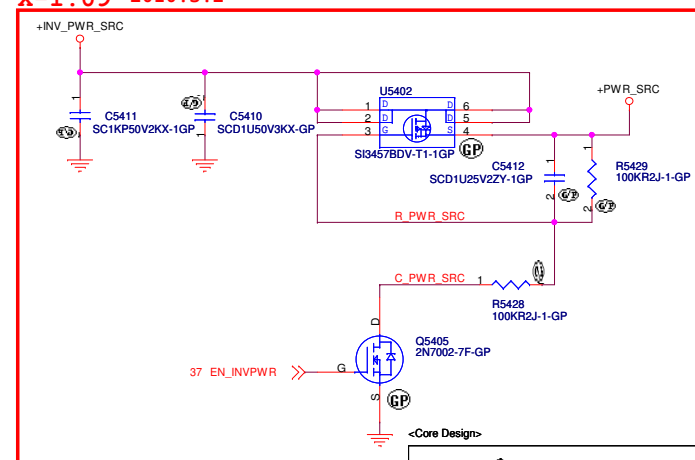
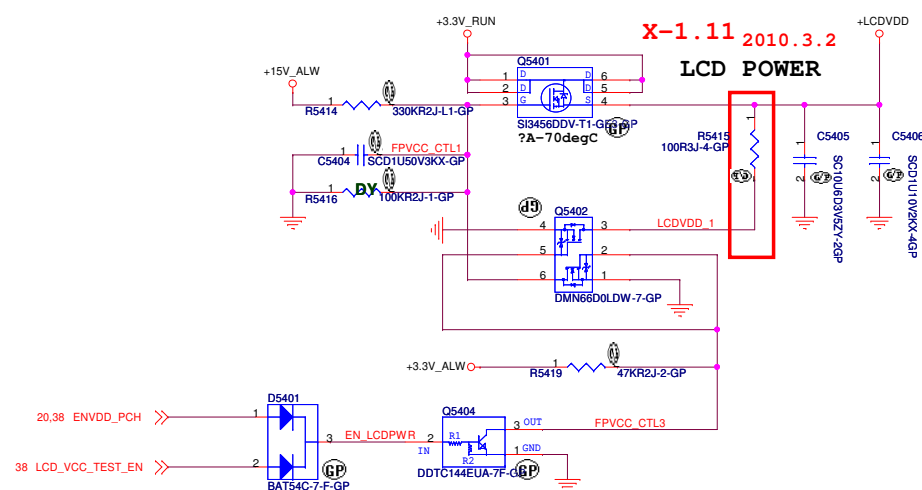
www.aitech1.ru

SSID = VIDEO

SSID = Inverter

## LED BACKLIGHT CONVERTER POWER

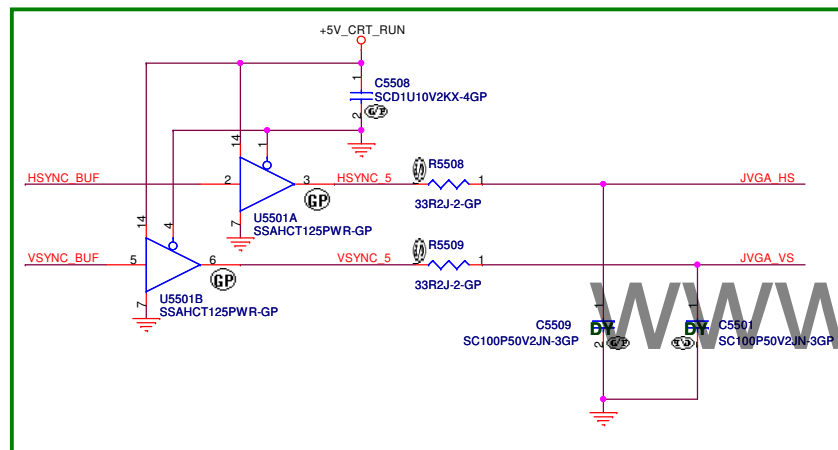
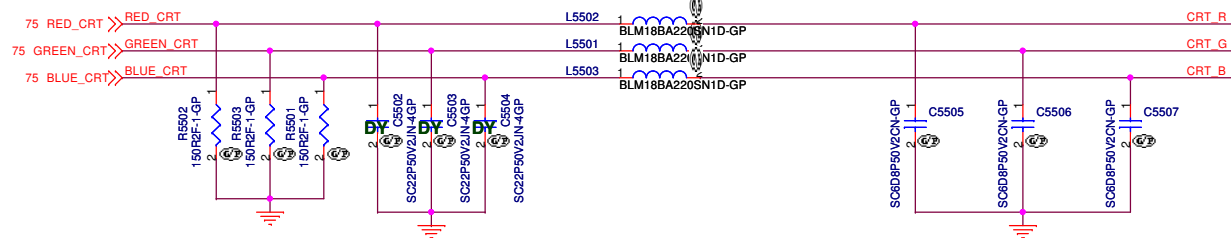
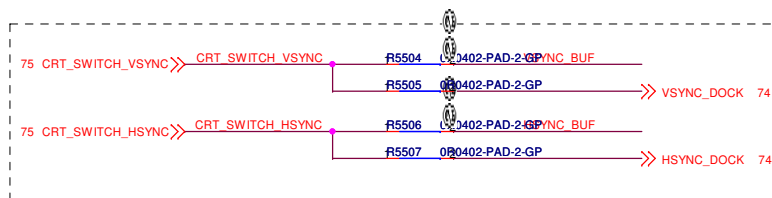
**X-1.09 2010.3.2**



**DELL** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

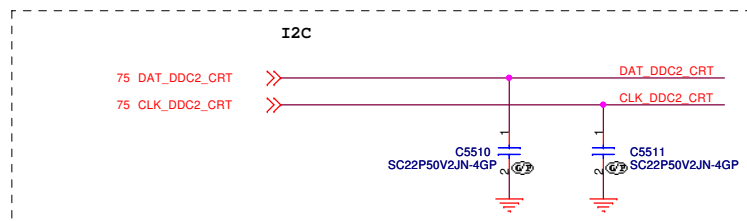
Title			
<b>LCD</b>			
Size	Document Number	Rev	
Custom	<b>Fonseca UMA</b>	X0	
Date:	Wednesday, March 17, 2010	Sheet	54 of 82

SSID = VIDEO

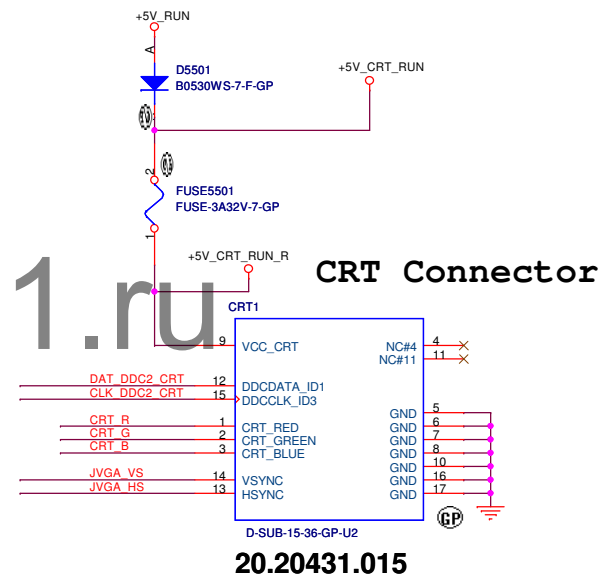


Layout Note:

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



MAX4885E has internal ESD protection and internal level shift



X-1.20 2010.3.10

AFTP5501 1 CRT\_R

<Core Design>



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Title

CRT

Size  
A3

Document Number

Fonseca UMA

Rev  
X02


Date: Thursday, March 18, 2010

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Fonseca UMA**

Date: Wednesday, March 10, 2010


Rev  
**X02**

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(Blank)

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserve***

Size A3	Document Number <i><b>Fonseca UMA</b></i>	Rev <i><b>X02</b></i>
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Date: <b>Wednesday, March 10, 2010</b>	Sheet <b>57</b> of <b>82</b>
--	------------------------------

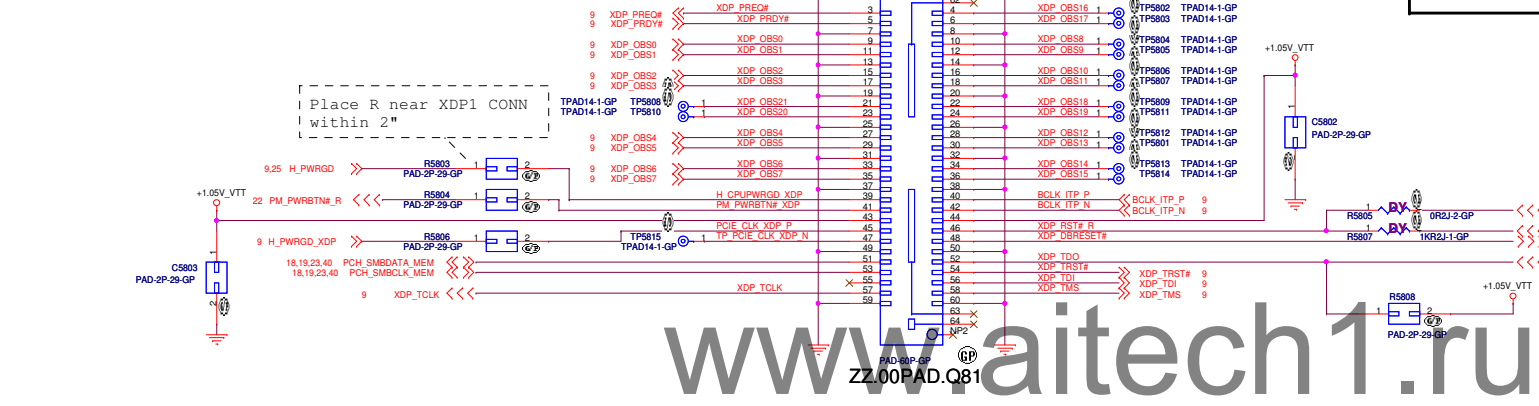
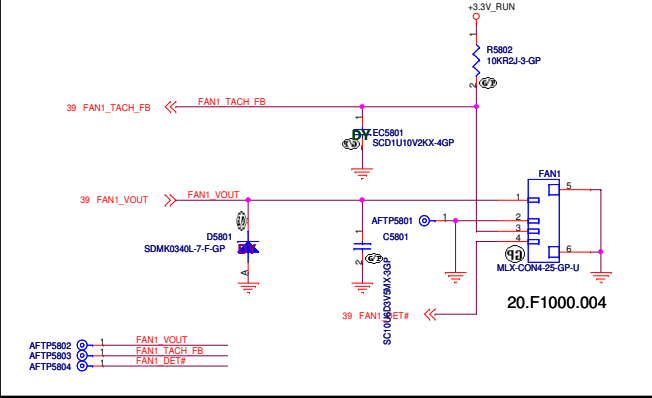
SSID = CPU X-1.02 2010.3.2

LOCATION	POP P/N	DY P/N
XDP1, XDP2	20.F0971.060	ZZ.00PAD.Q81
C5802	78.10421.2FL	ZZ.00PAD.Q71
C5803	78.10421.2FL	ZZ.00PAD.Q71
R5803	63.10234.1DL	ZZ.00PAD.Q71
R5804	63.R0034.1DL	ZZ.00PAD.Q71
R5806	63.R0034.1DL	ZZ.00PAD.Q71
R5808	63.51034.1DL	ZZ.00PAD.Q71

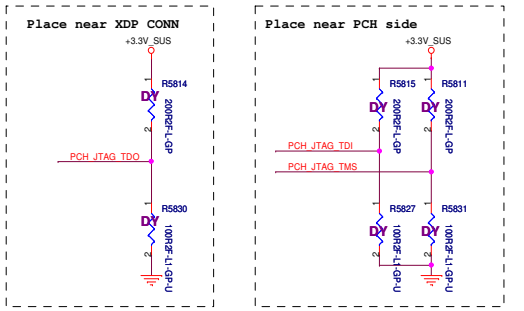
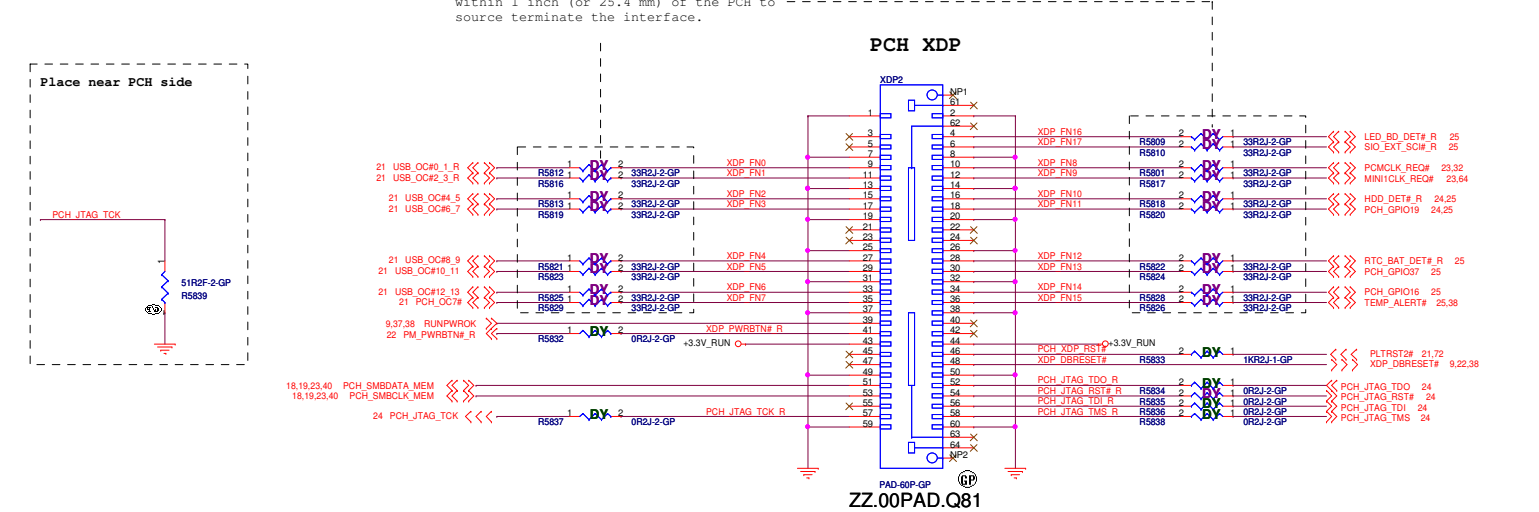
X-1.12 2010.3.10

LOCATION	POP P/N	DY P/N
TP5801~TP5815	ZZ.PAD14.001	ZZ.00PAD.Q91

SSID = Thermal

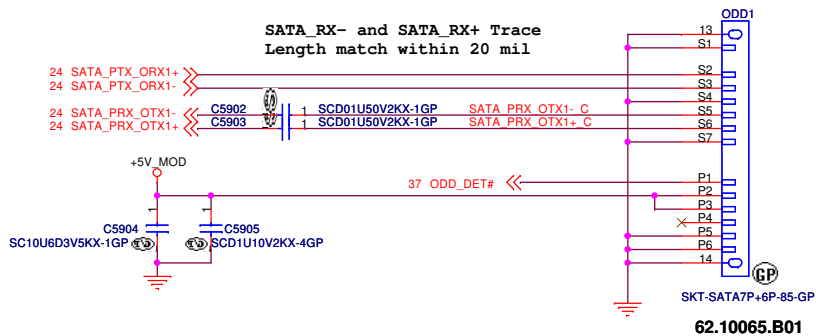


SSID = PCH

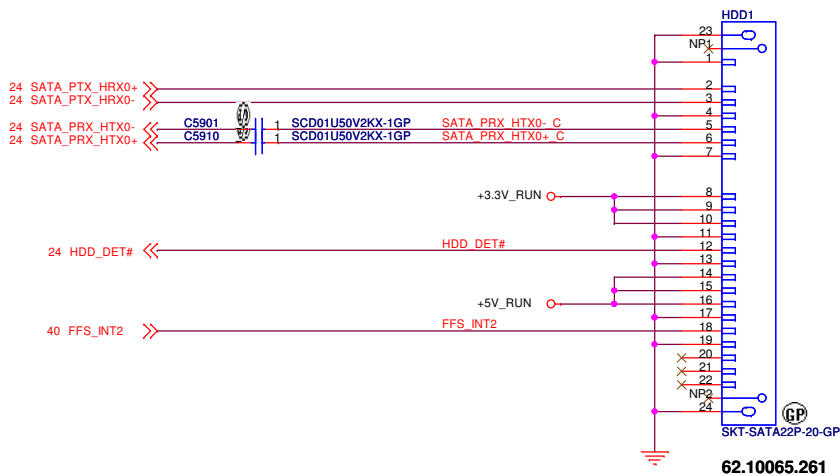




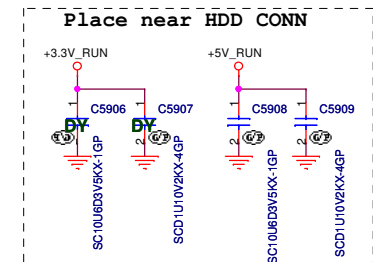
# SSID = SATA SATA ODD Connector



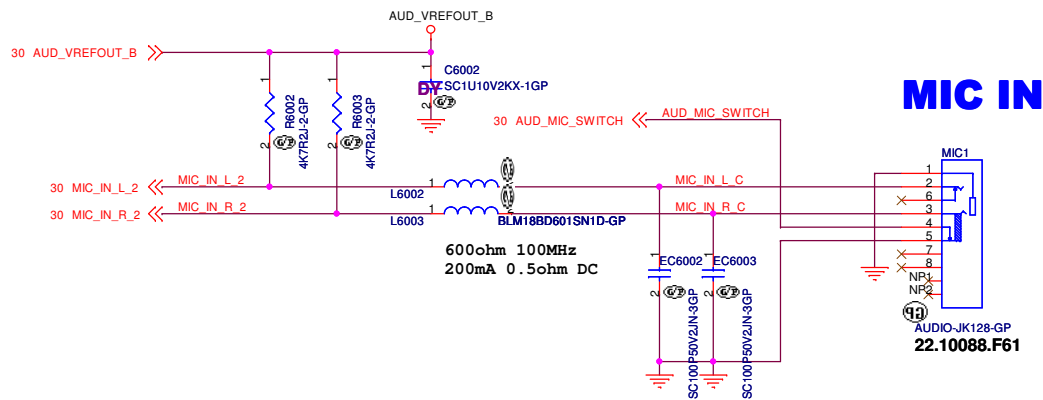
# SSID = SATA SATA HDD Connector



SATA HDD Interface comment  
\*\*\*\*\*  
--- GND  
RX+  
RX-  
TX-  
TX+  
--- GND  
\*\*\*\*\*  
----- 3.3V  
----- 3.3V  
----- 3.3V  
--- GND  
--- GND / Dell Detected Pin  
--- GND  
----- 5V  
----- 5V  
----- 5V  
--- GND  
(Dell: FFS\_INT for supported HDD)  
--- GND  
----- 12V (No support)  
----- 12V (No support)  
----- 12V (No support)  
\*\*\*\*\*

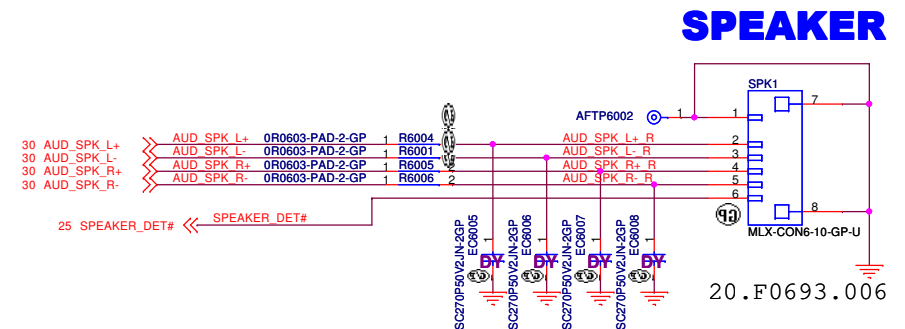


SSID = AUDIO



MIC IN

SSID = AUDIO

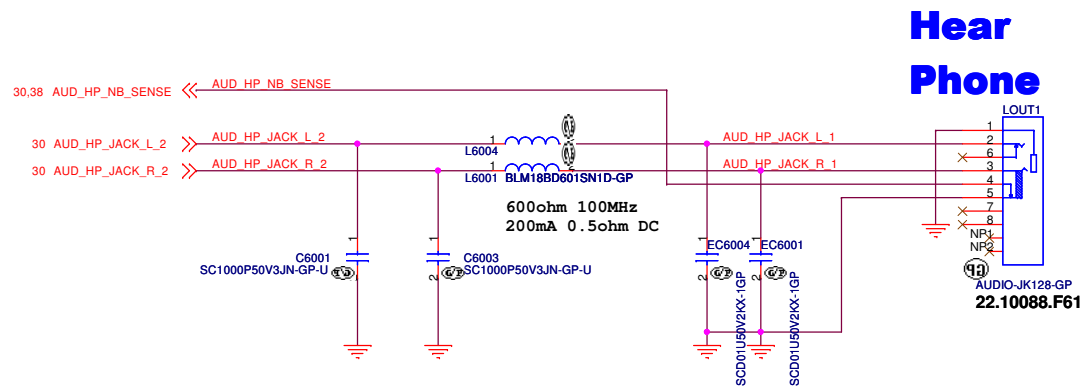


SPEAKER

AFTP6003 AUD SPK L+ R  
AFTP6004 AUD SPK L- R  
AFTP6005 AUD SPK R+ R  
AFTP6001 AUD SPK R- R  
AFTP6006 SPEAKER\_DET#

SSID = AUDIO

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Hear  
Phone

<Core Design>

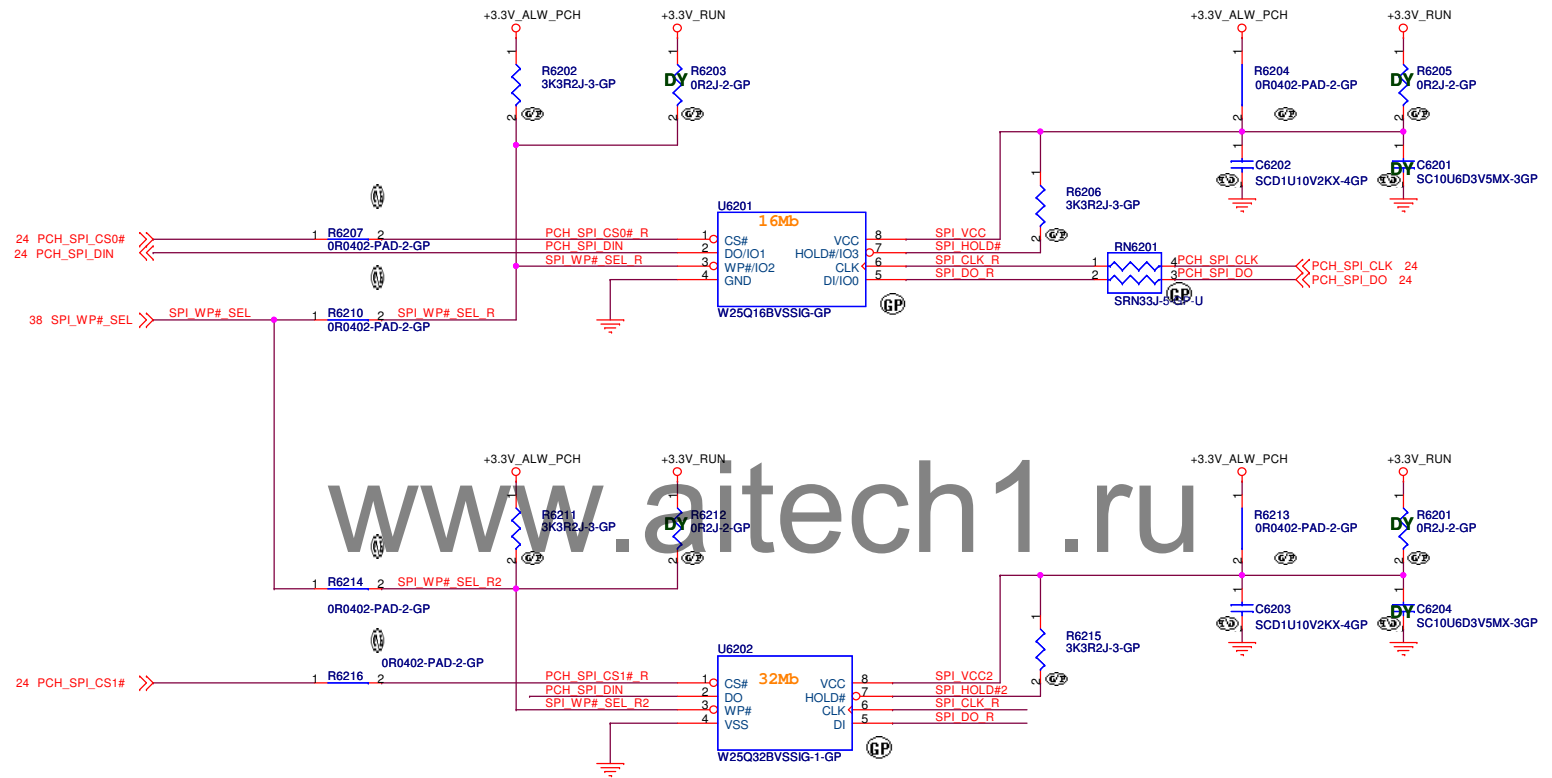
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**Audio Jack / Speaker Connector**  
Size A3 Document Number  
**Fonseca UMA** Rev  
**X02**  
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SSID = LOM

(Blank)  
www.aitech1.ru

SSID = Flash.ROM



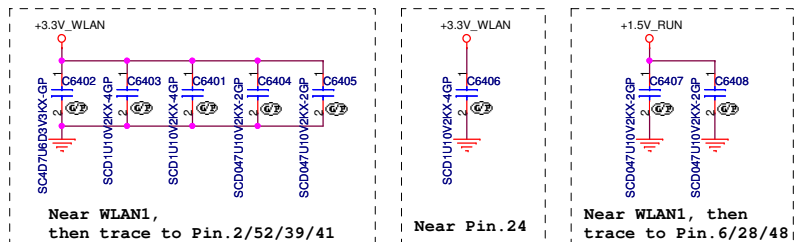
- #1 source: 72.25Q16.001 (2MB, Winbond)  
#2 source: 72.25165.B01 (2MB, MXIC)  
#3 source: 72.02516.A01 (2MB, Numonyx)
- #1 source: 72.25Q32.A01 (4MB, Winbond)  
#2 source: 72.25325.A01 (4MB, MXIC)  
#3 source: 72.25P32.B01 (4MB, Numonyx)

Pin.2  
From Intel checklist,  
SPI\_CS0#/CS1#  
No series resistor required  
if routing length is 1.5"-6.5"  
(with 1 or 2 SPI device)

Pin.6  
Intel checklist  
No series resistor required if routing length is 1.5"-6.5"  
(with 1 or 2 SPI device)



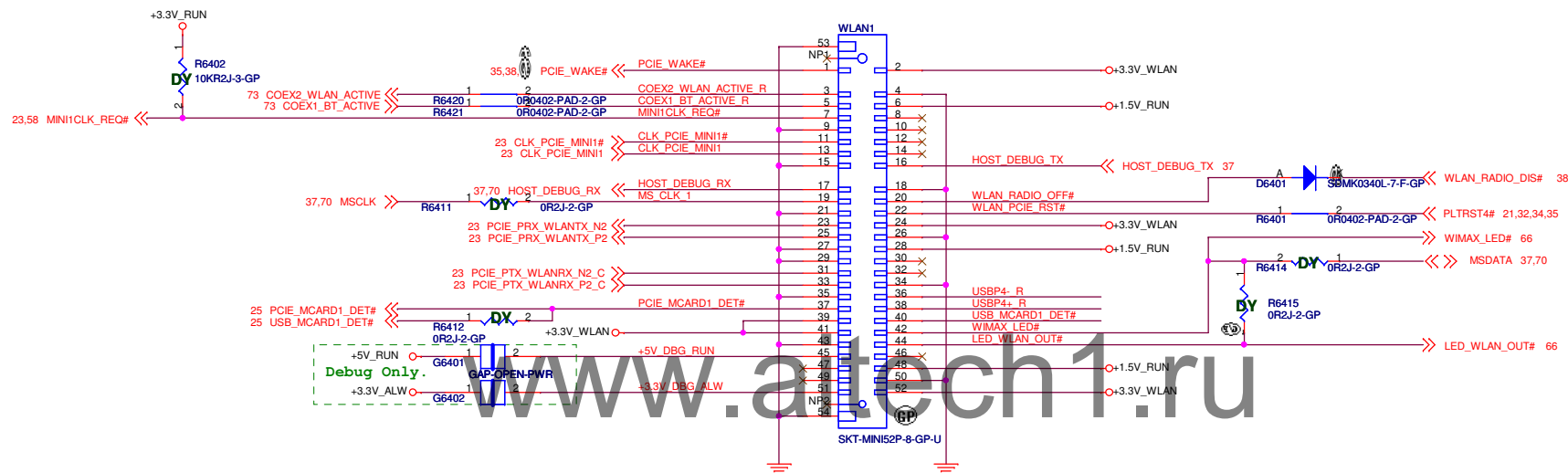
SSID = WLAN



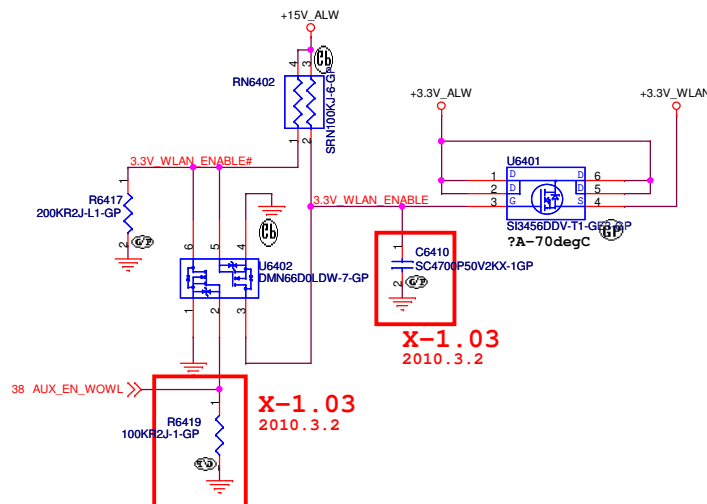
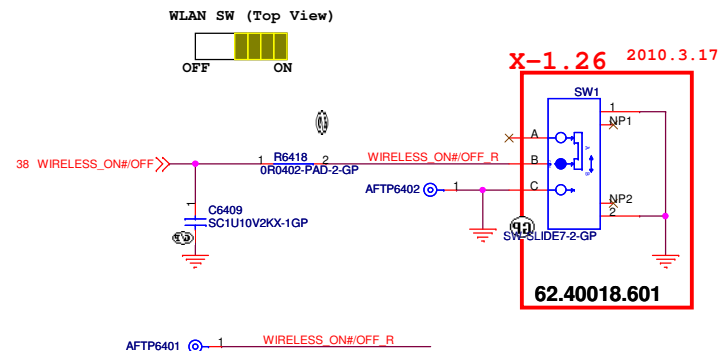
## DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	B44
17	HOST_DEBUG_RX	B46
19	8051_TX	B43
42	8051_RX	A40

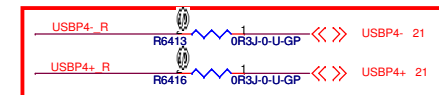
## MiniCard WLAN connector



## Wireless Switch



X-1.19 2010.3.10

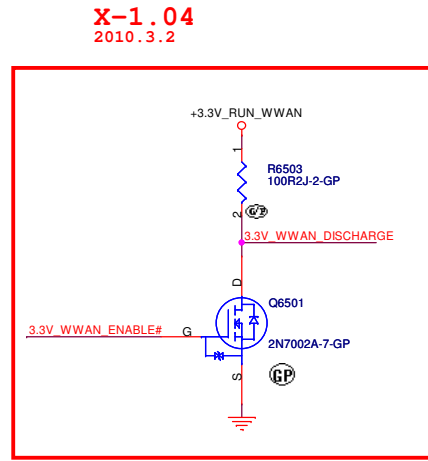
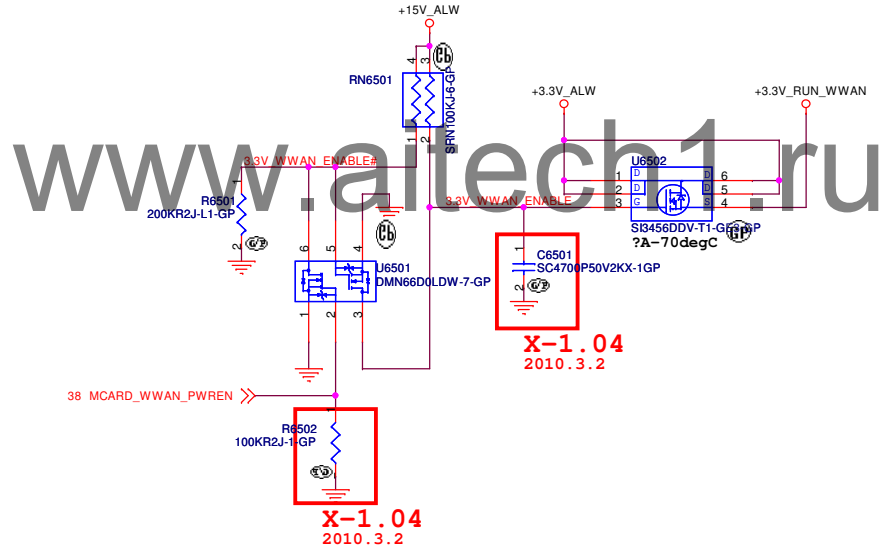
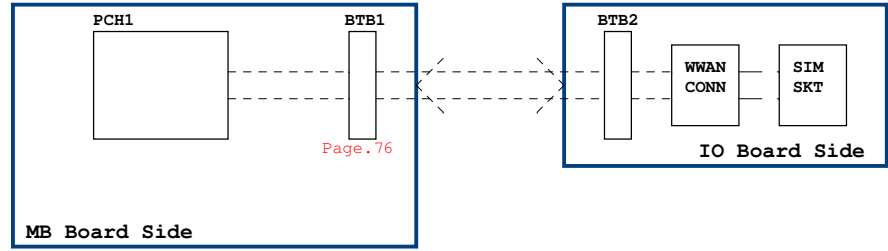


Close WLAN1

<Core Design>

<b>DELL</b> Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>WLAN / Serial Out Connector</b>	
Size Custom	Document Number <b>Fonseca UMA</b>
Date: Thursday, March 18, 2010	Sheet 64 of 82

SSID = WWAN

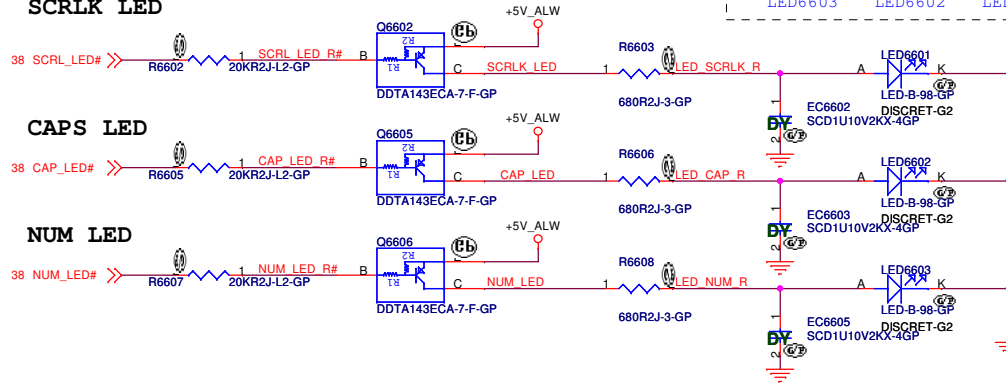


# SSID = User.interface

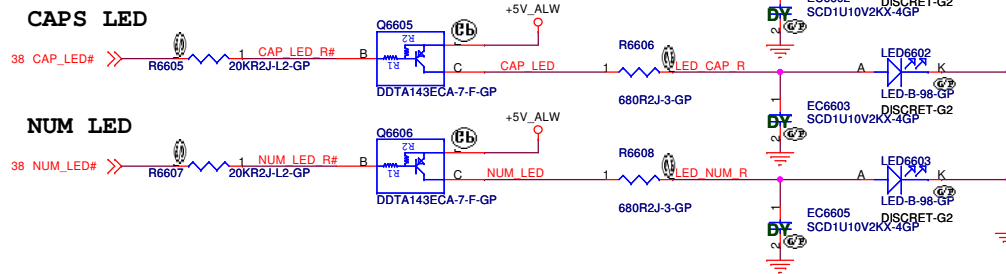
LED Location from left to right  
(MB, Top View)

NUM CAPS SCRLK  
LED6603 LED6602 LED6601

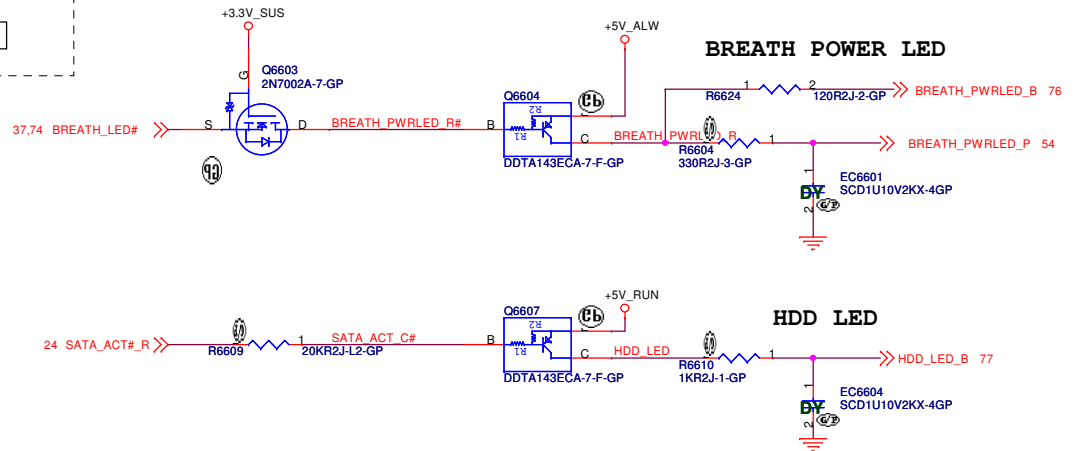
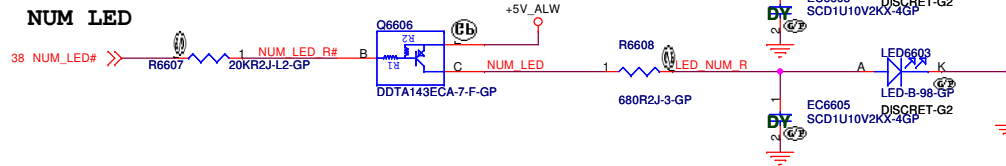
## SCRLK LED



## CAPS LED

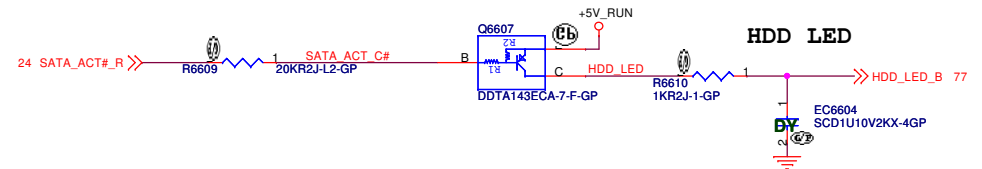


## NUM LED

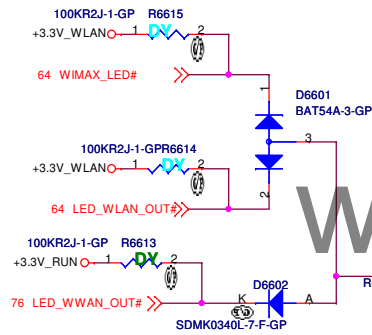


## BREATH POWER LED

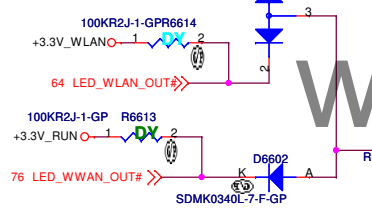
## HDD LED



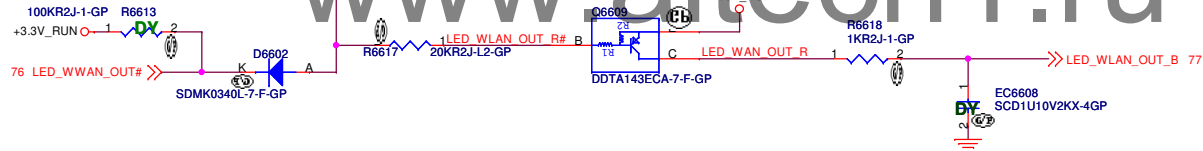
## WIMAX LED



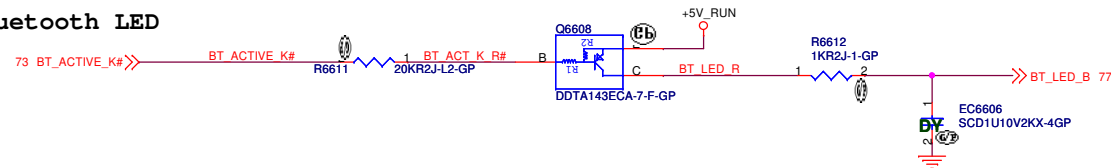
## WLAN LED



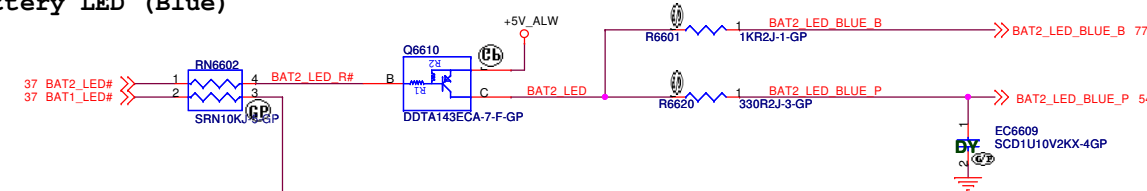
## WWAN LED



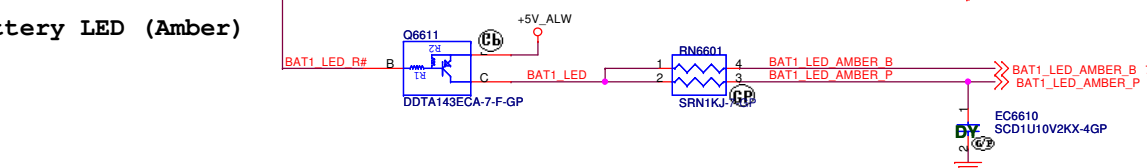
## Bluetooth LED



## Battery LED (Blue)



## Battery LED (Amber)

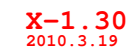


<Core Design>

<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>LED</b>		
Size A3	Document Number <b>Fonseca UMA</b>	Rev <b>X02</b>
Date: Wednesday, March 17, 2010	Sheet 66	of 82



**SSID = SmartCard**

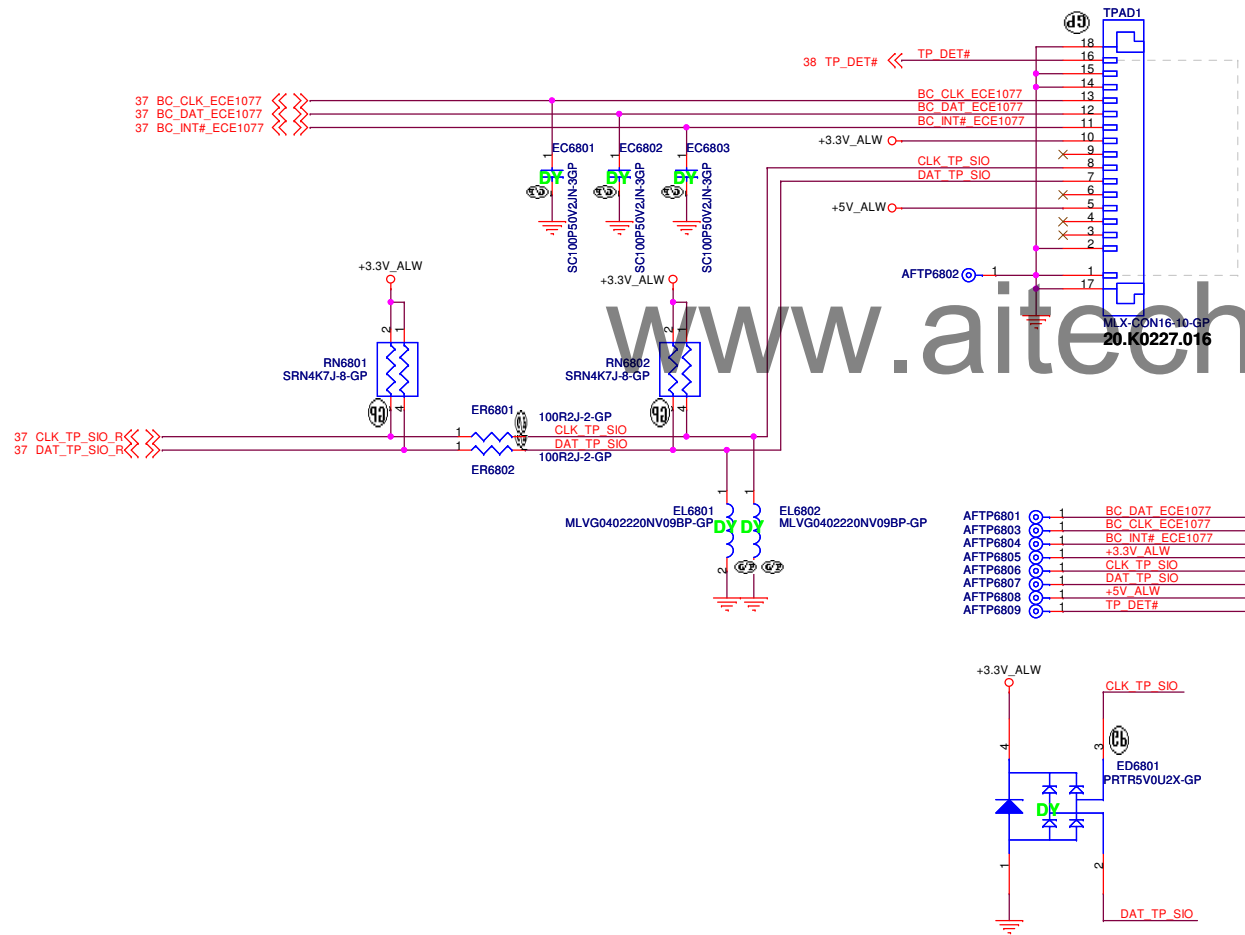


<b><i>Smart Card Socket</i></b>					
Size A3	Document Number <b><i>Fonseca UMA</i></b>				Rev <b><i>X02</i></b>
Date:	Friday, March 19, 2010	Sheet	67	of	82

<b><i>Smart Card Socket</i></b>					
Size A3	Document Number <b><i>Fonseca UMA</i></b>				Rev <b><i>X02</i></b>
Date:	Friday, March 19, 2010	Sheet	67	of	82

SSID = Touch.Pad

## TouchPad Connector



### Touch PAD Module Side

16	TP_DET#
15	GND
14	GND
13	BC_CLK (ECE1077)
12	BC_DAT (ECE1077)
11	BC_INT# (ECE1077)
10	3.3V_ALW
09	3.3V_RUN (Internal NC)
08	PS2_CLK
07	PS2_DATA
06	5V_RUN (Backlight, No Use)
05	5V_ALW (Chip change to use 3V, NC)
04	PWM (Backlight, No Use)
03	GND (Backlight, No Use)
02	GND
01	Diag_loop

<Core Design>



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Title

**Touch Pad Connector**

Size  
A3

Document Number

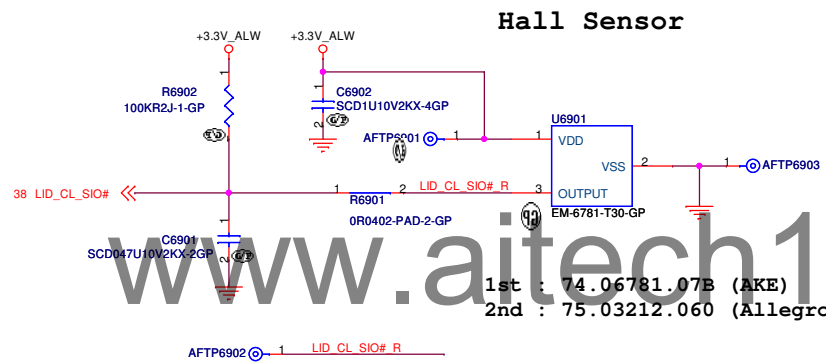
**Fonseca UMA**

Rev  
**X02**

Date: Thursday, March 18, 2010

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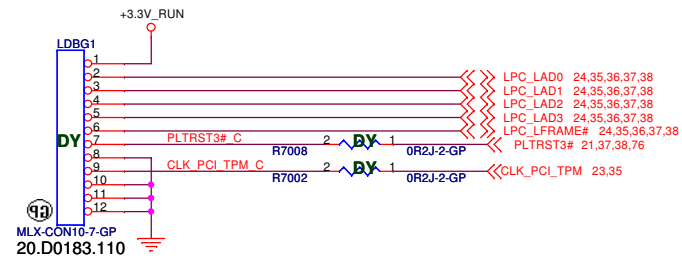
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2nd : 75.03212.060 (Allegro)

SSID = User.Interface

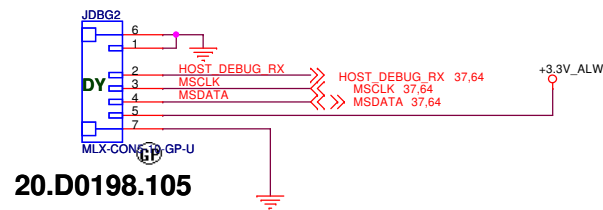
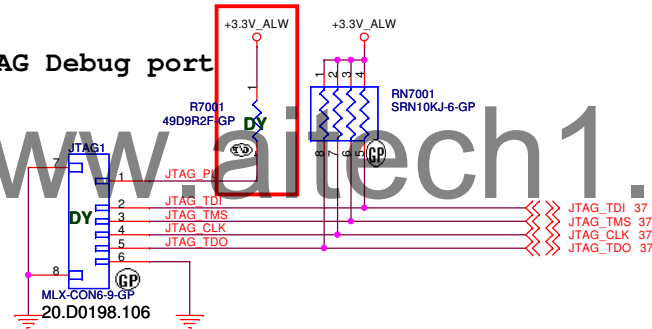
### LPC Debug port



LDBG1, need pop R7008, R7002

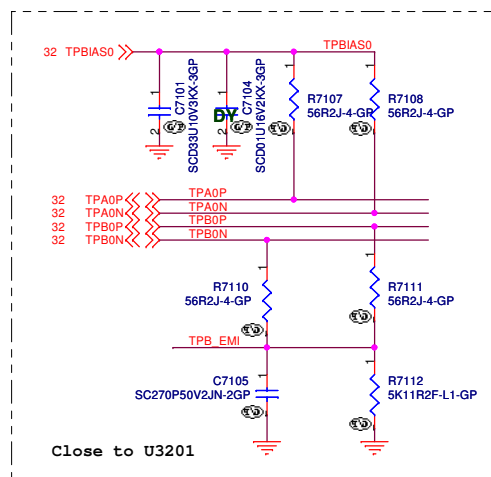
X-1.22 2010.3.10

### JTAG Debug port



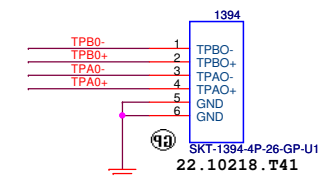
<Core Design>

SSID = 1394



Pinout diagram for the 8-pin connector of the TPA01 module. The diagram shows a central 8-pin connector with pins numbered 1 through 8. The pinout is as follows:

Pin	Signal	Color
1	TPB0N	Blue
2	TPB0P	Blue
3	TPA0N	Red
4	TPA0P	Red
5	R7106	Blue
6	R7101	Blue
7	R7109	Blue
8	R7113	Blue

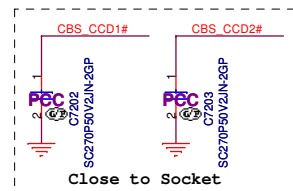


Shield GND separately for pairs of  
TPA+ & TPA- and TPB+ & TPB-

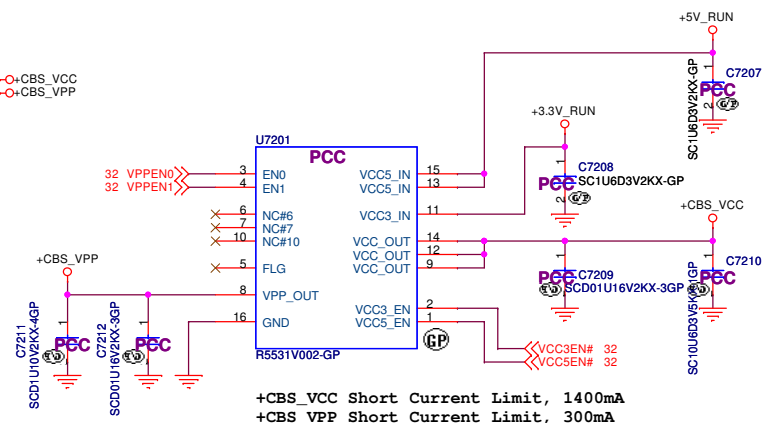
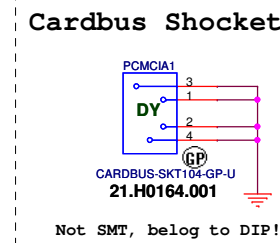
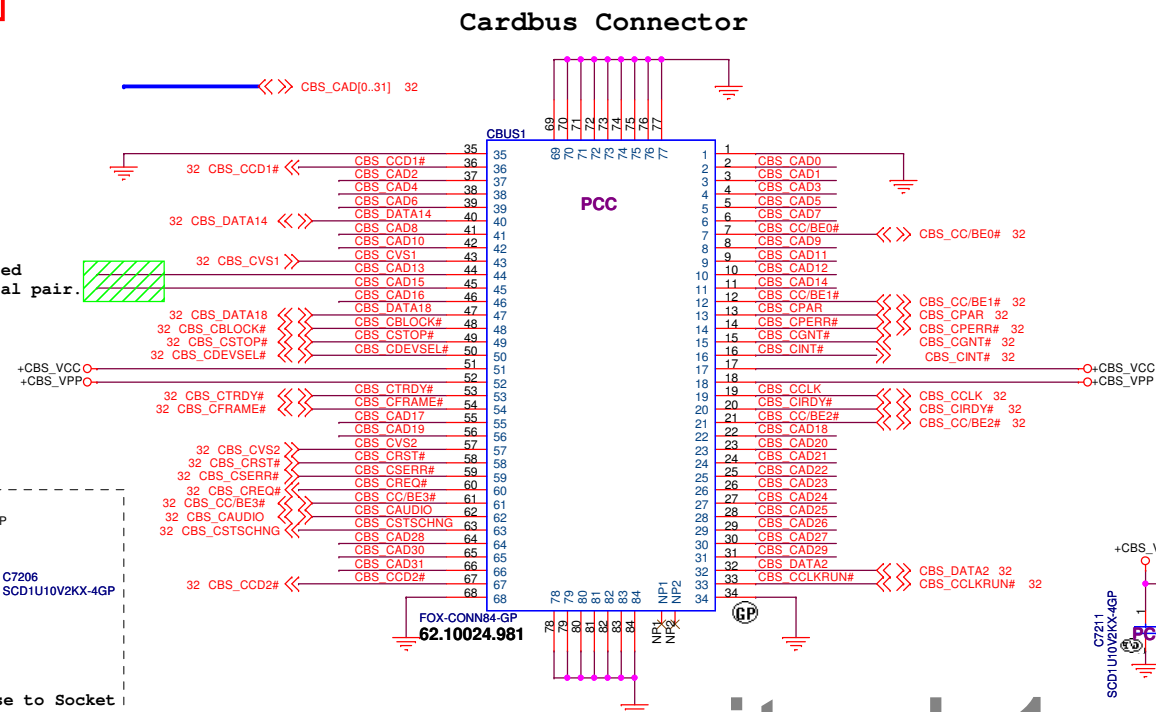
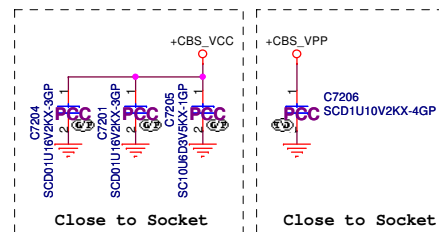
**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>1394 Connector / Flash Socket</b>			
Size	Document Number	Rev	
A3	<b>Fonseca UMA</b>	<b>X02</b>	
Date:	Wednesday, March 17, 2010	Sheet	71 of 82

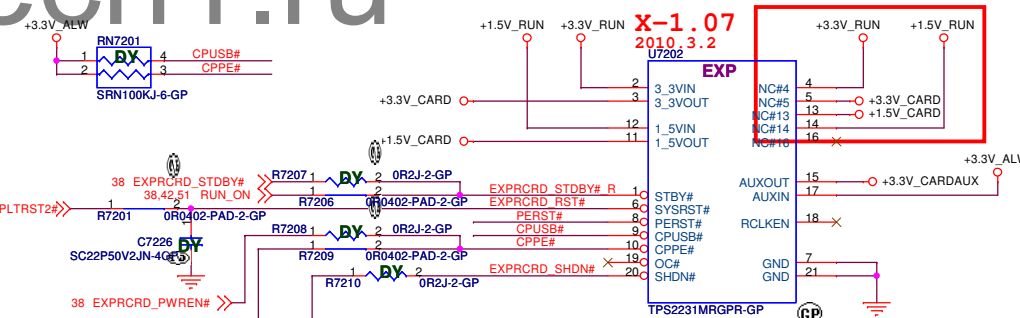
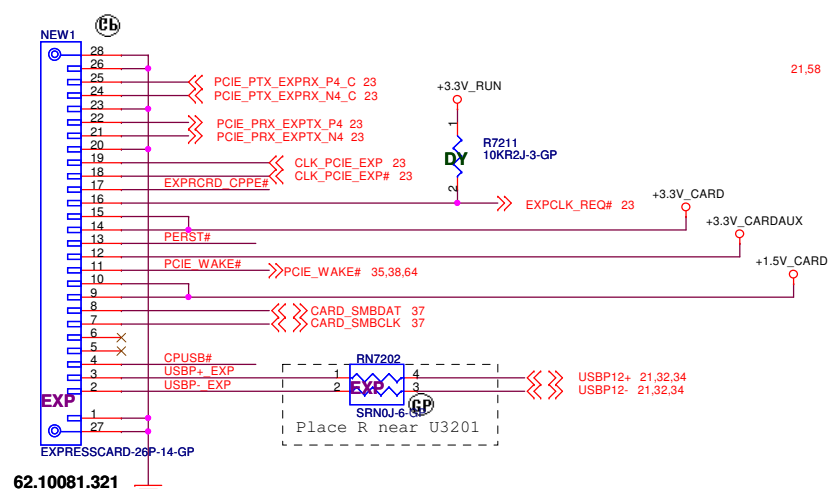
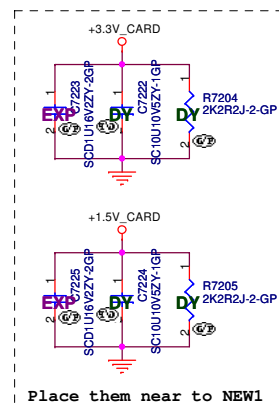
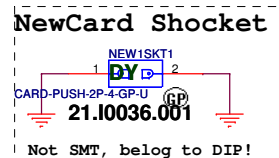
**SSID = CARDBUS**



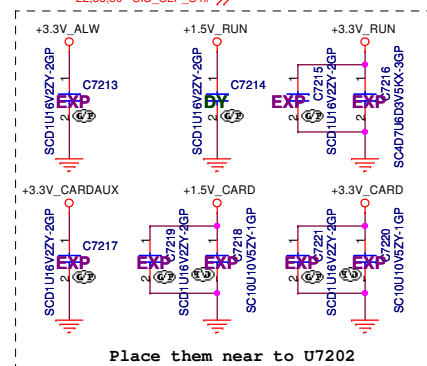
CBS\_CAD13, CBS\_CAD15 Can be used  
as Express Card USB differential pair.



```
SSID = ExpressCard
```

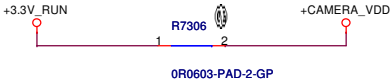


+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA

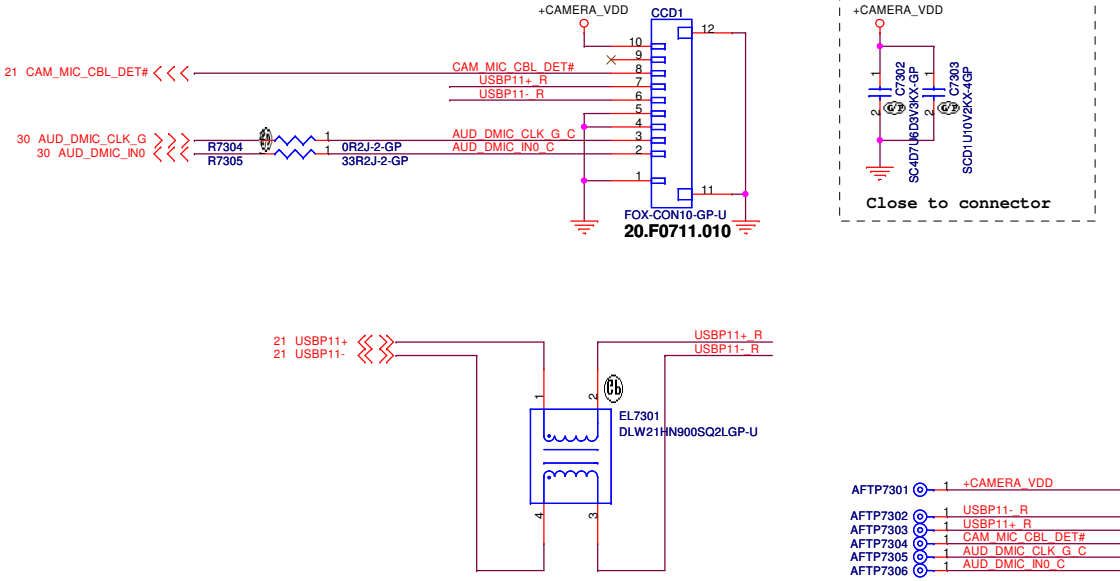


SSID = User.interface

Camera Power CTRL



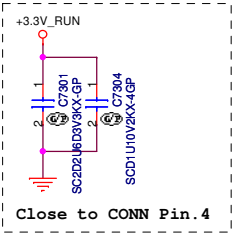
Camera Connector



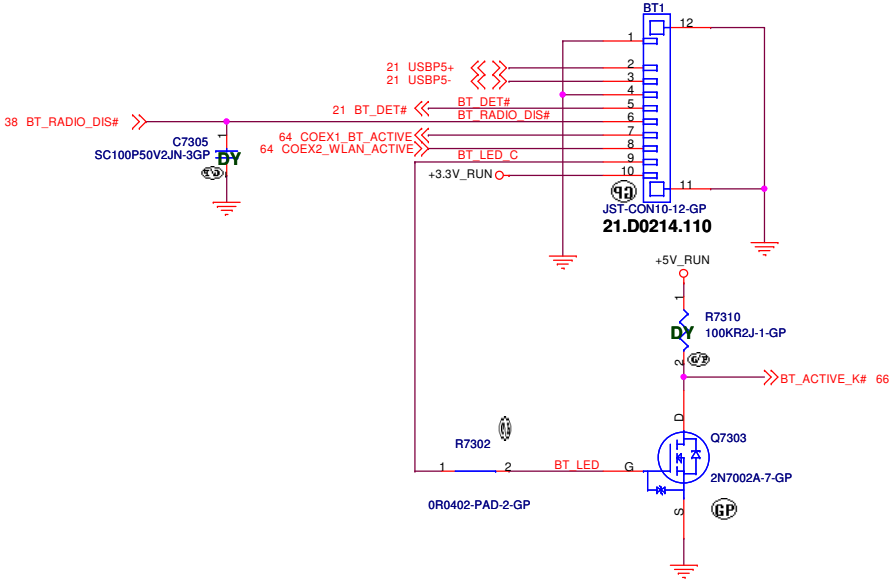
SSID = User.interface

www.aitech1.ru

Bluetooth Connector



- AFTP7307 1 +3.3V\_RUN
- AFTP7308 1 COEX1\_BT\_ACTIVE
- AFTP7309 1 COEX2\_WLAN\_ACTIVE
- AFTP7310 1 USBP5+
- AFTP7311 1 BT\_RADIO\_DIS#
- AFTP7312 1 BT\_LED
- AFTP7313 1 BT\_DET#
- AFTP7314 1 BT\_DET#



MB BT CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V
11	NC		
12	NC		

<Core Design>

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Title  
**Bluetooth / Camera / DMIC**

Size A3 Document Number  
**Fonseca UMA**

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**Clost to DKL**

**D7401**

Pin	Signal	IC Pin	Signal
1	DPC DOCK AUX SW	10	DY TMSD <sub>2</sub> , D2+
2	DPC DOCK AUX SW#	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DPC DOCK CA DET	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DPC DOCK HPD	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DPC DOCK HPD	6	TMSD <sub>1</sub> , D1+

**IP4280CZ10-GP**

**D7402**

Pin	Signal	IC Pin	Signal
1	DPB DOCK AUX SW	10	DY TMSD <sub>2</sub> , D2+
2	DPB DOCK AUX SW#	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DPB DOCK CA DET	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DPB DOCK HPD	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DPB DOCK HPD	6	TMSD <sub>1</sub> , D1+

**IP4280CZ10-GP**

**DOCK LOW TRD0+**

**DOCK LOW TRD0-**

**DOCK LOW TRD1+**

**DOCK LOW TRD1-**

**DOCK LOW TRD2+**

**DOCK LOW TRD2-**

**DOCK LOW TRD3+**

**DOCK LOW TRD3-**

**C7408**

Pin	Signal	IC Pin	Signal
1	DOCK LOW TRD0+	10	DY TMSD <sub>2</sub> , D2+
2	DOCK LOW TRD0-	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DOCK LOW TRD1+	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DOCK LOW TRD1-	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DOCK LOW TRD2+	6	TMSD <sub>1</sub> , D1+
6	DOCK LOW TRD2-	5	DOCK LOW TRD3+
7	DOCK LOW TRD3+	4	DOCK LOW TRD3-
8	DOCK LOW TRD3-	3	DOCK LOW TRD0+
9	DOCK LOW TRD0+	2	DOCK LOW TRD0-
10	DOCK LOW TRD0-	1	DOCK LOW TRD1+

**IP4280CZ10-GP**

**DOCK LOW TRD0+**

**DOCK LOW TRD0-**

**DOCK LOW TRD1+**

**DOCK LOW TRD1-**

**DOCK LOW TRD2+**

**DOCK LOW TRD2-**

**DOCK LOW TRD3+**

**DOCK LOW TRD3-**

**C7408**

Pin	Signal	IC Pin	Signal
1	DOCK LOW TRD0+	10	DY TMSD <sub>2</sub> , D2+
2	DOCK LOW TRD0-	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DOCK LOW TRD1+	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DOCK LOW TRD1-	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DOCK LOW TRD2+	6	TMSD <sub>1</sub> , D1+
6	DOCK LOW TRD2-	5	DOCK LOW TRD3+
7	DOCK LOW TRD3+	4	DOCK LOW TRD3-
8	DOCK LOW TRD3-	3	DOCK LOW TRD0+
9	DOCK LOW TRD0+	2	DOCK LOW TRD0-
10	DOCK LOW TRD0-	1	DOCK LOW TRD1+

**IP4280CZ10-GP**

**DOCK LOW TRD0+**

**DOCK LOW TRD0-**

**DOCK LOW TRD1+**

**DOCK LOW TRD1-**

**DOCK LOW TRD2+**

**DOCK LOW TRD2-**

**DOCK LOW TRD3+**

**DOCK LOW TRD3-**

**C7408**

Pin	Signal	IC Pin	Signal
1	DOCK LOW TRD0+	10	DY TMSD <sub>2</sub> , D2+
2	DOCK LOW TRD0-	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DOCK LOW TRD1+	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DOCK LOW TRD1-	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DOCK LOW TRD2+	6	TMSD <sub>1</sub> , D1+
6	DOCK LOW TRD2-	5	DOCK LOW TRD3+
7	DOCK LOW TRD3+	4	DOCK LOW TRD3-
8	DOCK LOW TRD3-	3	DOCK LOW TRD0+
9	DOCK LOW TRD0+	2	DOCK LOW TRD0-
10	DOCK LOW TRD0-	1	DOCK LOW TRD1+

**IP4280CZ10-GP**

**DOCK LOW TRD0+**

**DOCK LOW TRD0-**

**DOCK LOW TRD1+**

**DOCK LOW TRD1-**

**DOCK LOW TRD2+**

**DOCK LOW TRD2-**

**DOCK LOW TRD3+**

**DOCK LOW TRD3-**

**C7408**

Pin	Signal	IC Pin	Signal
1	DOCK LOW TRD0+	10	DY TMSD <sub>2</sub> , D2+
2	DOCK LOW TRD0-	9	NC#10 TMSD <sub>2</sub> , NC#2
3	DOCK LOW TRD1+	8	TMSD <sub>2</sub> , GND TMSD <sub>2</sub> , VDD
4	DOCK LOW TRD1-	7	NC#7 TMSD <sub>1</sub> , NC#5
5	DOCK LOW TRD2+	6	TMSD <sub>1</sub> , D1+
6	DOCK LOW TRD2-	5	DOCK LOW TRD3+
7	DOCK LOW TRD3+	4	DOCK LOW TRD3-
8	DOCK LOW TRD3-	3	DOCK LOW TRD0+
9	DOCK LOW TRD0+	2	DOCK LOW TRD0-
10	DOCK LOW TRD0-	1	DOCK LOW TRD1+

**IP4280CZ10-GP**

**DOCK LOW TRD0+**

**DOCK LOW TRD0-**

**DOCK LOW TRD1+**

**DOCK LOW TRD1-**

**DOCK LOW TRD2+**

**DOCK LOW TRD2-**

**DOCK LOW TRD3+**

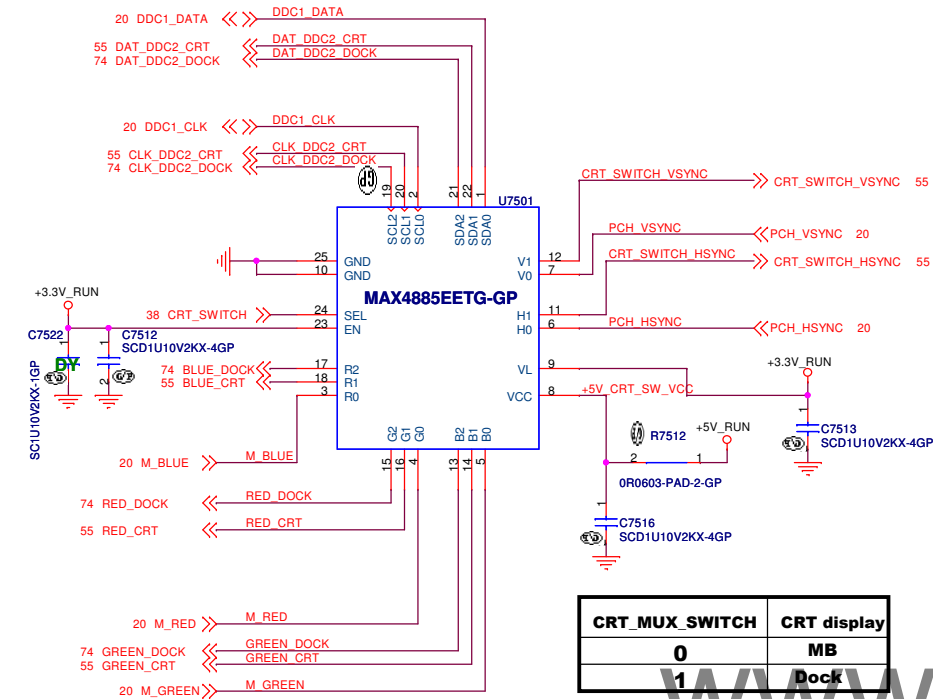
**DOCK LOW TRD3-**

**C7408**

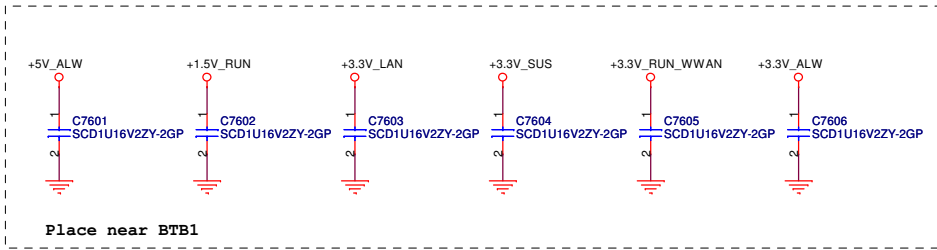
Pin	Signal
-----	--------



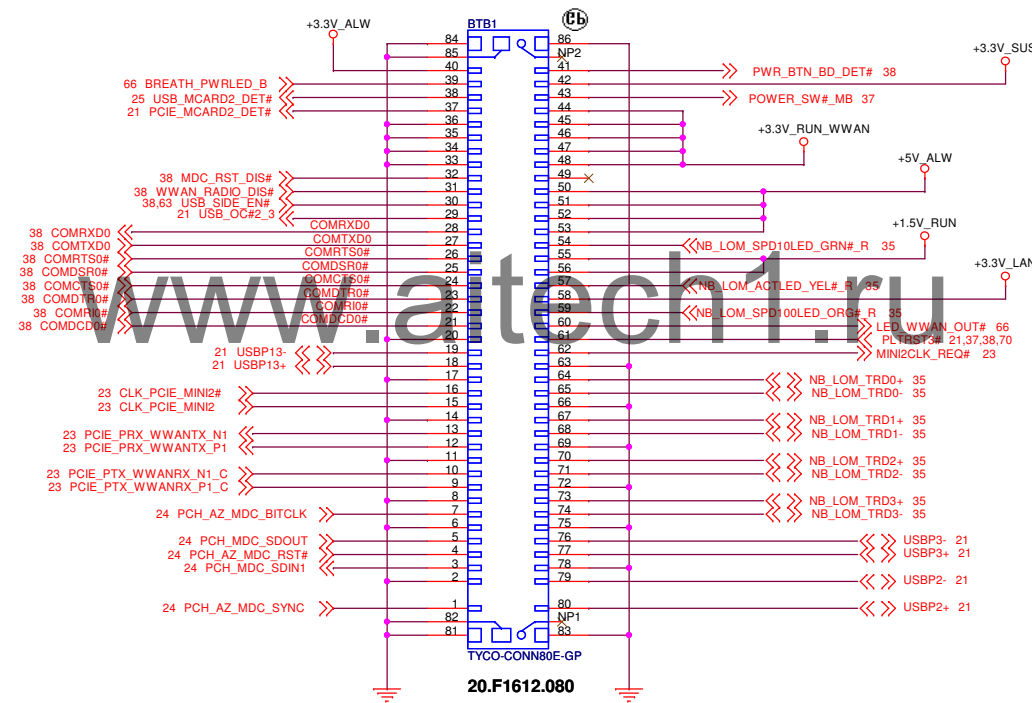
## SSID = DOCK CRT SWITCH



# SSID = User.Interface



## IO Board Connector



<Core Design>



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Title

**IO Board CONN**

Size  
A3

Document Number

**Fonseca UMA**

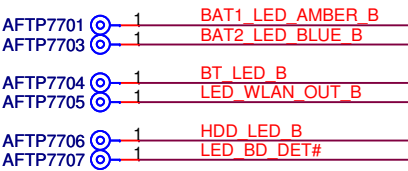
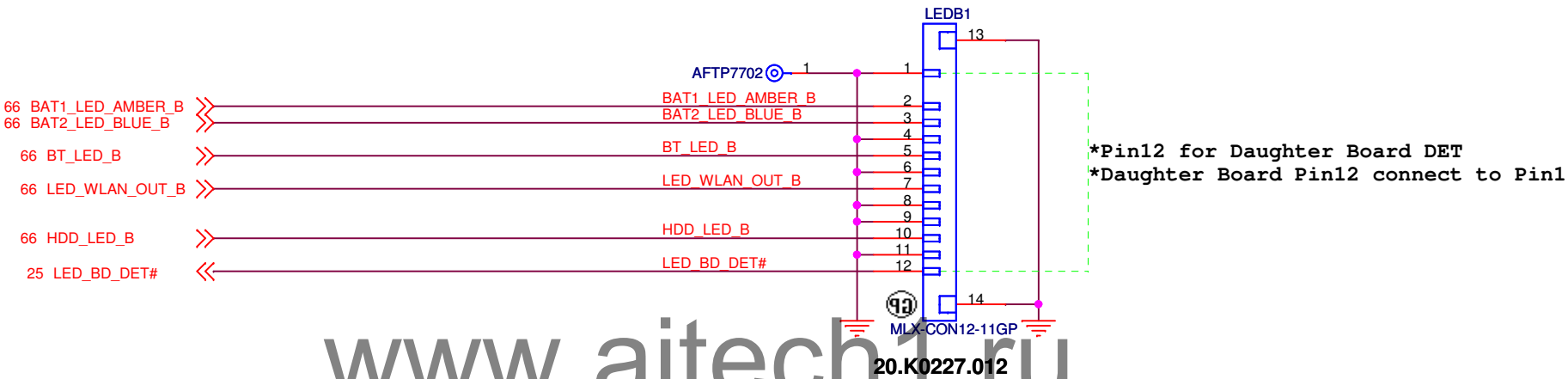
Rev  
X02

Date: Wednesday, March 17, 2010

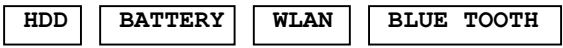
Sheet 76 of 82

SSID = User.interface


LED BD Connector



LED Location from left to right



<Core Design>



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Title

**LED Board Connector**

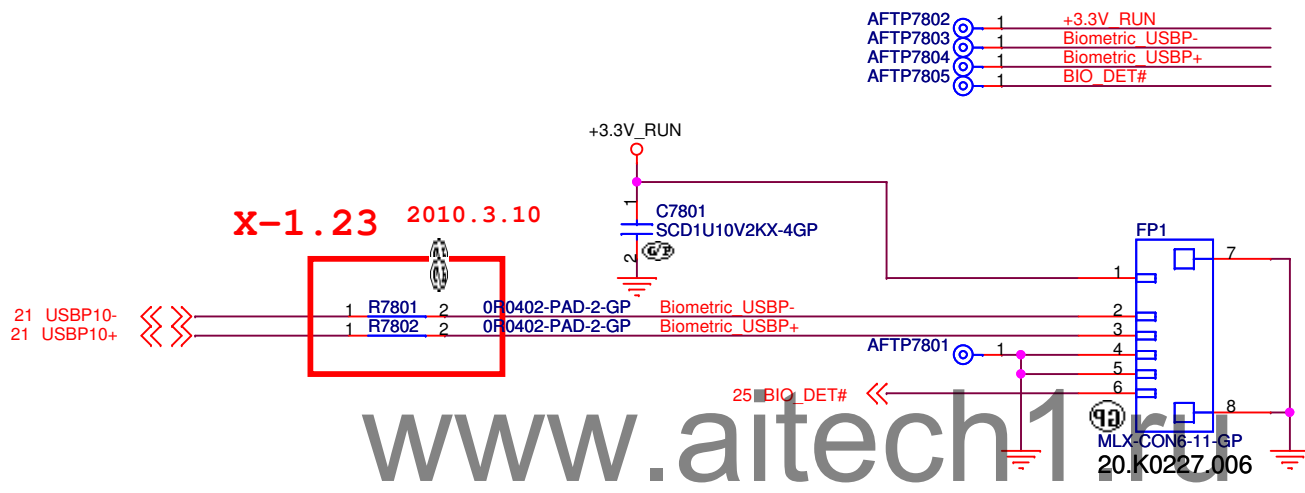
Size  
A4

Document Number  
**Fonseca UMA**

Rev  
**X02**


Date: Thursday, March 18, 2010Sheet 77 of 82

SSID = User.Interface



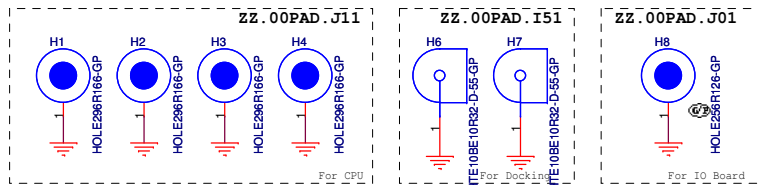
Biometric Connector

<Core Design>

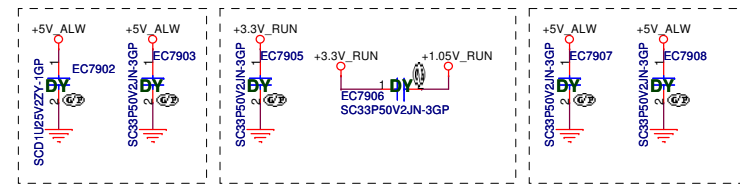
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Title <b>Finger Printer Board CONN</b>			
Size A4	Document Number <b>Fonseca UMA</b>		Rev <b>X02</b>
Date: Thursday, March 18, 2010		Sheet 78 of 82	

# SSID = Mechanical

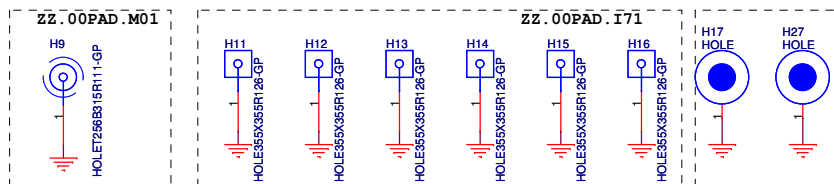
Hole



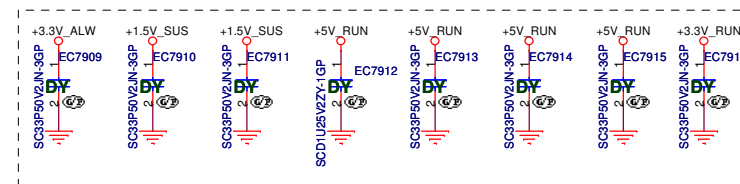
RF Cap.



Hole

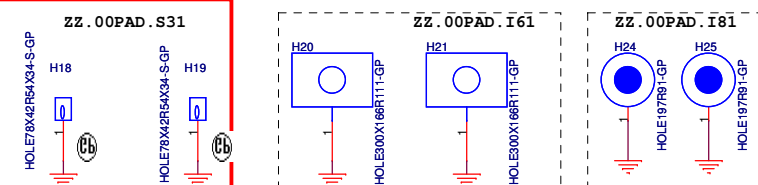


RF Cap.

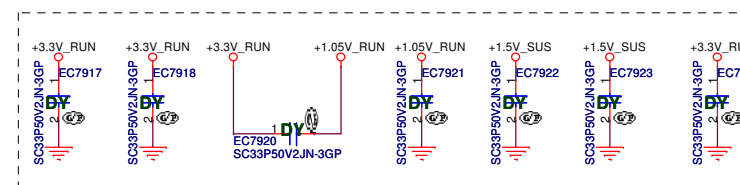


Hole

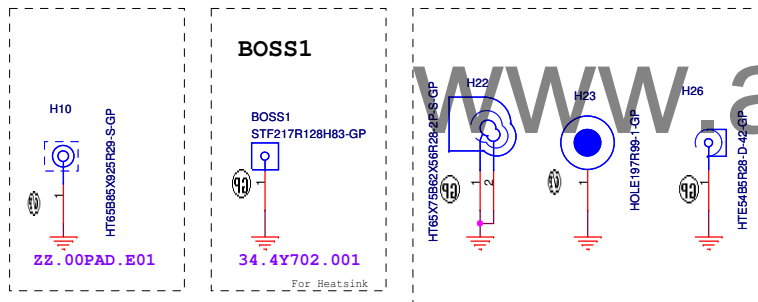
X-1.27  
2010.3.17



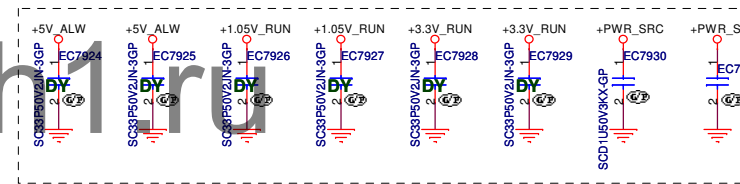
RF Cap.



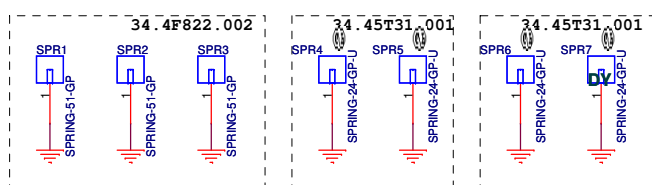
Hole



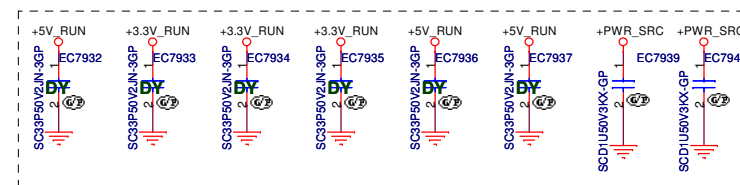
RF Cap.



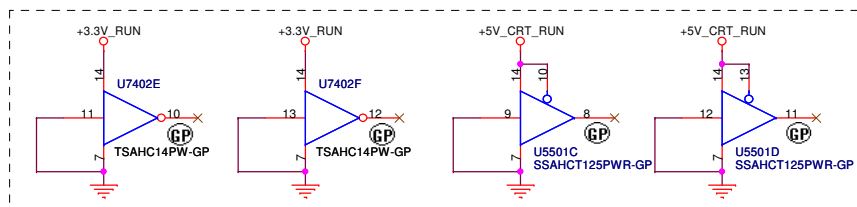
Spring



EMI Cap.



Unused Parts



EMI Cap.

<Core Design>

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Title  
**Unused Parts / EMI RF Cap.**  
Size A3 Document Number  
Date: Thursday, March 18, 2010 Sheet 79 of 82

DATE	NO	PAGE	ACTION	reference	Issue Description	OWNER
20100302	X-1.01	47	change	PTC4701 --->DY PTC4702 --->POP	change cap place location for factory request.	EE
	X-1.02	58	DY	XDP1,XDP2,C5802,C5803,R5803,R5804,R5806,R5808	change to DY part number for layout used.	EE
	X-1.03	64	STUFF	C6410,R6419	C6410 --> soft start R6419 --> quick discharge	EE
	X-1.04	65	STUFF	C6501,R6502,R6503,Q6501	C6501 --> soft start R6502,R6503,Q6501 --> quick discharge	EE
	X-1.05	42	Change	C4208	change to 470P for soft start used	EE
	X-1.06	51	ADD	PC5108	reserve location	POWER-EE
	X-1.07	72	ADD	U7202	add pin4,5,13,14 for second source	EE
	X-1.08	37	Change	R3703	change board ID to -1	EE
	X-1.09	37, 54	ADD	R3741,Q5404,R5428,R5429,C5412,U5402,C5410,C5411	add power switch to control lcd power	EE
	X-1.10	71	remove	L7504,L7101	remove co-layout part for PSE request	EMC
20100310	X-1.11	54	change	R5415	change part number to 63.10133.15L	EE
	X-1.12	58	change	TP5801~TP5815	change test pad to DY part for layout	EE
	X-1.13	7	remove	RN701,RN703,RN704,RN705	remove 0 ohm part for layout	EE
	X-1.14	23	change	RN2312,RN2313	change RN2312 ,RN2313 to short pad for layout	EE
	X-1.15	23	remove	RN2307,RN2308,RN2301	remove 0 ohm part for layout	EE
	X-1.16	25	remove	RN2501	remove 0 ohm part for layout	EE
	X-1.17	32	change	RN3201	change RN3210 to short pad for layout	EE
	X-1.18	40	STUFF	C4002		EE
	X-1.19	64	remove	EL6401	remove EL6401 for PSE request because it co-layout with resister.	PSE
	X-1.20	55	ADD	AFTP5501	add test pad for I/O test used	factory
	X-1.21	67	STUFF	C6704,C6705		EE
	X-1.22	70	DY	R7001	not use debug port	EE
	X-1.23	78	change	remove EL7801 change R7801,R7802 to short pad	remove EL7801 for PSE request because it co-layout with resister.	PSE
20100317	X-1.24	67	change	SC1 SC1SKT1	change connector type	ME
	X-1.25	63	remove	EL6301 EL6302	remove co-layout 0 ohm pad	PSE
	X-1.26	64	change	SW1	change connector type	PSE
	X-1.27	79	change	H18 H19	change hole type	ME
20100318	X-1.28	9	DY	R913 Q901 C901 R903		EE
	X-1.29	67	ADD	C6706		EE
20100319	X-1.30	67	change	C6704 C6705 R6705	change resister and capacitance value	EE

Core Design:

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Change List (1/1)</b>			
Size A3	Document Number <b>Fonseca UMA</b>		Rev <b>-1</b>
Date: Friday, March 19, 2010		Sheet 80	of 82